A Fully-Integrated Reconfigurable Dual-Band Transceiver for Short Range Wireless Communications in 180nm CMOS

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***Abstract*—A fully-integrated reconfigurable dual-band (760-960MHz and 2.4-2.5GHz) transceiver (TRX) for short range wireless communications is presented. The TRX consists of two individually-optimized RF front-ends for each band and one shared power-scalable analog baseband. The Sub-GHz receiver has achieved the maximum 75dBc 3rd-order harmonic rejection ratio (HRR3) by inserting a Q-enhanced notch filtering RF amplifier (RFA). In 2.4GHz band, a single-ended-to-differential RFA with gain/phase imbalance compensation is proposed in the receiver. A Σ-Δ fractional-N PLL frequency synthesizer with two switchable Class-C VCOs is employed to provide the LOs. Moreover, the integrated multi-mode PAs achieve the output P1dB (OP1dB) of 16.3dBm and 14.1dBm with both 25% PAE for Sub-GHz and 2.4GHz bands, respectively. A power-control loop is proposed to detect the input signal PAPR in real-time and flexibly reconfigure the PA's operation modes to enhance the back-off efficiency. With this proposed technique, the PAE of the Sub-GHz PA is improved by ×3.24 and ×1.41 at 9dB and 3dB back-off powers, respectively, and the PAE of the 2.4GHz PA is improved by ×2.17 at 6dB back-off power. The presented transceiver has achieved comparable or even better performance in terms of noise figure, HRR, OP1dB and power efficiency compared with the state-of-the-art.**

***Index Terms*—CMOS, wireless transceiver, RF, reconfigurable, HRR, power amplifier, PAPR, back-off efficiency enhancement.**

I. INTRODUCTION

The rapid evolution of healthcare electronics [1]-[2], smart home [3] and machine-to-machine communications [4] leads to the prosperous development in short range wireless communication systems. In medical caring sensor networks for pre-hospital and ambulatory emergency care, wireless connectivity replaces the cumbersome wired devices and benefits the real-time medical data collection [5]. In the smart home, wireless communication systems facilitate efficient management of utility services and offer convenient remote control to transfer command messages. All these applications have the common requirements of variable data rates and low power consumption.

Unlicensed ubiquitous access is always strongly desired for these applications. Besides the worldwide 2.4GHz band (2.4-2.5GHz), the Sub-GHz (760-960MHz) ISM-band has also been defined in China, EU, North America and Japan [6]. The reconfigurable chip supporting both the Sub-GHz and 2.4GHz bands offers the best solution in terms of flexibility and interoperability among various devices and networks, and the appropriate protocol can be chosen to optimize power consumption in numerous applications scenarios where data throughput varies dramatically.

There exist many technical challenges in the implementation of a low-power and low-cost reconfigurable dual-band transceiver. Firstly, previously reported transceivers for short range wireless communications mainly only support the single-band operation [7]-[10], or sacrifice some performance with one wideband TRX path to cover dual bands [10]-[11]. In these transceivers, the active Gilbert cells are employed to realize the frequency conversion [8]-[9], [11]-[12], which limits the linearity and 1/f noise performance, and the out-of-band (OB) interference rejection issue in the receiver is also neglected. In this work, a flexible Zero-IF/Low-IF reconfigurable architecture including two individually-optimized RF front-ends for each band and one shared power-scalable analog baseband is adopted to address the different design challenges in Sub-GHz and 2.4GHz bands, and the passive up/down-conversion mixers clocked by differentiated duty-cycle LOs are employed to improve the linearity and noise performance with low power consumption. The Sub-

GHz receiver forms the 4-path filter with the passive voltage mixer driven by 25% duty-cycle LOs to enhance the OB attenuation; the 2.4GHz receiver enhances the OB attenuation by using a low noise amplifier (LNA) with the LC tuned load, and the passive voltage mixer driven by 50% duty-cycle LOs is used to achieve the comparable OB rejection with lower power consumption. However, compared with the architecture employing the single wide-band Gilbert mixer [13] which provides some gain to suppress the noise from the following stages, the presented architecture would require the higher gain LNA (RFA) and consume the higher chip area.

Secondly, since the off-chip antenna is single-ended in most wireless systems, a balun is needed to realize the single-ended-to-differential (S2D) conversion in the receiver [13]-[14]. The passive off-chip balun is usually employed for its superiority in wideband coverage. However, compared with the bulky and lossy passive off-chip balun, an active on-chip balun is more attractive for its low cost. In this work, a gain-boosting balun-LNA is employed in Sub-GHz band to suppress the noise contribution from the following stages, and a balun-RFA with gain/phase imbalance compensation is introduced in 2.4GHz band to reduce the loss, reject the second-order distortion and the common-mode noise. The drawback is that the architecture based on active balun makes the single dual-band antenna inapplicable.

The third challenge is the 3rd-order harmonic rejection (HRR3) issue for the Sub-GHz operation. Jeffery A. Weldon, et.al has proposed the harmonic rejection transmitter by employing the harmonic rejection mixer technique [15] to tackle the problem. However, the scheme based on the harmonic rejection mixer needs eight-phase LOs which are usually generated from one PLL frequency synthesizer operating at 4 times of the operation frequency and would consume huge power in 0.18um CMOS. Moreover, extra gain/phase calibration is needed to compensate the mismatch in order to achieve high harmonic rejection rate. Although the two-stage harmonic rejection technique that is less insensitive to the mismatch has been exploited in [16]-[17] to achieve high HRR3 performance, the design complexity has been increased greatly. In this work, a Q-enhanced notch filtering RFA along with the 4-path filter is proposed to improve the HRR3 in Sub-

GHz band.

The forth challenge is to integrate highly efficient and linear power amplifiers (PAs) on-chip. Since most short range communications, such as 802.11ah draft, utilize OFDM modulation with high Peak-to-Average-Power-Ratio (PAPR) to achieve higher throughputs, the PA should operate efficiently not only at peak output power but also at the back-off power to improve the average efficiency and prolong the battery lifetime. The Doherty PA is a popular scheme to obtain high back-off efficiency [18]-[19], but the onset of the auxiliary PA is poorly defined. The transformer-based power-combiner dual-mode PA [20] improves the average efficiency by turning off one of the stages, but the area overhead is large. Moreover, the power control loop to realize the mode-switching automatically is not mentioned in [20]. A multi-mode PA in SiGe process using integrated varactor-based tunable matching networks [21] is proposed to enhance the back-off efficiency. However, it is difficult to get high Q (>100@2GHz) varactors in CMOS process, and the mode-switching through tuning the varactors is implemented manually, too. In this work, multi-mode CMOS PAs with the power-control loops are proposed to enhance the back-off efficiency.

Besides, peak detector based RF-AGC (automatic gain control) and differential-RSSI (received signal strength indicator) based baseband-AGC are both integrated to extend the receiver dynamic range. Class-C VCOs are adopted in the Σ-Δ fractional-N PLL frequency synthesizer to enhance the phase noise performance with low power consumption.

The remainder of this paper is organized as follows. Section II describes the architecture of the dual-band transceiver. More details on the circuit implementations are discussed in Section III. Section IV reports the measured results, and finally some conclusions are drawn in Section V.

II. TRANSCEIVER ARCHITECTURE

Fig. 1 shows the block diagram of the proposed reconfigurable dual-band transceiver [22], where two individually-optimized RF front-ends and one shared power-scalable analog baseband are employed to address the design challenges in Sub-GHz and 2.4GHz bands while minimizing the area overhead. The receiver can be configured into Zero-IF architecture for wideband applications

(BW=10MHz) to reduce the power or Low-IF architecture for narrowband applications (f_{IF}=3MHz, BW=1MHz/2MHz) to avoid the performance degradation caused by 1/f noise and DC offsets, and the transmitter adopts the direct up-conversion architecture. In order to save the power, 25% and 50% duty-cycle LO generators are adopted to drive the passive voltage mixers in Sub-GHz and 2.4GHz bands, respectively. Besides, digitally-assisted calibration blocks, such as DC offset cancellation (DCOC), I/Q imbalance calibration, automatic gain control (AGC) and automatic frequency control (AFC) are all integrated to enable a practical chip. The SPI interface is utilized to reconfigure the transceiver operation modes. The bandgap-based bias circuit provides various biases for the transceiver and the power supplies are regulated with on-chip LDOs.

A. Receiver Architecture

In Sub-GHz band, a balun-LNA with wideband input matching is employed to realize the S2D conversion. In wideband mode, the direct conversion architecture with the passive voltage mixer clocked by 25% duty-cycle LOs is adopted to achieve the 4-path OB filtering characteristic through impedance translation [23]; in narrowband mode, the capacitance C_1 (Fig.1) would be reconfigured into a low value (~0.5pF) to achieve the flat in-band gain while sacrificing some OB attenuation. Since the expensive SAW filter with steep band-pass filtering effect is inapplicable for low-cost design, the 3rd-order harmonics located at 2.28-2.88GHz would enter into the receiver path and degrade the noise and linearity performance; however, the 5th-order harmonics located at 3.8-4.8GHz or the higher-order harmonics are far away from the operation band and could be attenuated sufficiently due to the limited LNA bandwidth (15dB rejection for 5th-order harmonic) and 4-path filtering. The transmission power of 2.4GHz WiFi is about 20dBm occupying 22MHz bandwidth which induces 16.5dBm equivalent noise in 10MHz bandwidth. The application scenarios define the distance between the WiFi hot spot and the proposed short range wireless communication node as about 10m, in which the WiFi signal attenuation would be 60dB according to the free-space path loss equation. Therefore, the strength of the received 3rd-order harmonic interference is defined as -40dBm with 3.5dB margin. In order to attenuate the interference of -

40dBm down to the noise floor, .e.g. -102dBm in 10MHz BW mode with NF=5dB, an HRR3 of >62dBc is required. The simulation shows that the 4-path filter could only provide 14dB HRR3, and the achievable HRR3 in [24] is only 20dB, even with 4-path filtering subtraction technique and 65nm CMOS process. Thus, a Q-enhanced notch filtering RFA is proposed to help reject the 3rd-order harmonics while providing some amplification for the in-band signals.

In 2.4GHz band, a single-ended inductively source degenerated LNA with narrowband input matching and an LC tuned load interfaces with the antenna to provide some OB interferences rejection. The 2nd harmonics resulted from the single-ended LNA is sufficiently attenuated by the high-pass filter with the corner frequency of about 100MHz which is composed of the capacitors and resistors for the ac coupling between the LNA, RFA and the RFA, Mixer. A balun-RFA with gain/phase imbalance compensation is cascaded to realize the S2D conversion while rejecting the second-order distortion and common-mode noise. A passive voltage mixer with 50% duty-cycle LOs is adopted since unacceptable high power would be consumed to generate the 25% duty-cycle non-overlap 2.4GHz LOs in 180nm CMOS (the post-layout simulations show a rise/fall time of ~65ps due to the self-loading effect, and the 25% duty-cycle LO generator would consume 19mW power, 13.7mW higher than the 50% duty-cycle LO generator). It is more advantageous to utilize the 25% duty-cycle LOs in more advanced process, such as 65nm CMOS in [25]-[26], mainly due to the significant reduced transistor capacitance. Fig. 2 shows the simulated filtering characteristics at the 50% duty-cycle clocking mixer input with different capacitance C_1 @ f_{LO}=2.45GHz. In wideband mode, the capacitance C_1 would be configured as a low value (~0.1pF) to achieve the flat in-band gain; in narrowband mode, the unwanted maximum gain shift in the impedance translation [27] due to the parasitic capacitance at the RFA output is in turn utilized, and the reconfigurable capacitance C_1 is set to 5pF in maximum to enhance the OB attenuation and avoid the upper/lower sideband asymmetry issue.

Since the OB interferences may be strong and the OB attenuation provided by the RF front-end is not enough, the pressure on the OB linearity and cascaded noise performance are shifted to the

baseband. As shown in Fig. 1, a trans-conductance amplifier (TCA) followed by a 1st-order trans-impedance low-pass filter (TILPF) is employed to form the capacitive load for the mixers and calibrate the I/Q imbalance in the current domain. The reconfigurable capacitor array C_2 before the TILPF shorts the high-frequency current to the ground and further filters the OB interferences. Besides, a peak detector based RF-AGC is adopted to reasonably assign the gain settings of the LNA, RFA and TILPF to avoid saturating the following channel filter. The channel filter is a 1st/2nd/3rd-order Butterworth type with low-pass/complex band-pass operation modes. Furthermore, a differential RSSI-based baseband-AGC is employed to extend the receiver dynamic range.

B. Transmitter Architecture

In the transmitter, a direct up-conversion architecture with the passive voltage mixer is employed. Similar to the RX part, the 25% duty-cycle LOs are adopted to drive the passive mixer in Sub-GHz band to achieve high gain while the 50% duty-cycle LOs are used in 2.4GHz band to reduce the power consumption. 10-bit 32MS/s over-sampling DACs move the aliases far away from the desired band and alleviate the filtering requirements of analog baseband. A 2nd-order Tow-Thomas trans-impedance low-pass filter (TILPF) with reconfigurable bandwidth of 3/5/11MHz is introduced to reject the DAC aliases and out-of-band quantization noise, and its bandwidth is designed a little wider than the signal bandwidth to obtain flatter in-band group delay and better EVM performance. To boost the linearity and reduce the power consumption, a reconfigurable high slew-rate Class-AB op-amp with the trans-linear loop and programmable driving capability is utilized in the TILPF [28]. Then, a 1st-order passive LPF is cascaded to further filter the out-of-band noise. The over-sampling DACs together with the active-passive hybrid analog baseband attenuate the DAC aliases by 40dB and 65dB in wideband and narrowband modes, respectively. Finally, in order to support various modulation schemes with different PAPRs, two multi-mode Class-AB PAs are integrated for each band to obtain the optimized performance. Moreover, a novel power-control loop consisting of a power detector, comparators and digital control logic is introduced to flexibly reconfigure the PA's operation modes in real-time and

enhance the back-off efficiency. In this work, various digitally-assisted calibration blocks are integrated, including the digital I/Q calibration to reject the image, the data weighted averaging (DWA) algorithm to calibrate the DAC mismatch and the DCOC in front of the TILPF to suppress the LO leakage [29].

III. CIRCUITS IMPLEMENTATIONS

A. Receiver

1) Dual-Band RF Front-Ends

The Sub-GHz LNA is a gain-boosting common-gate common-source (CG-CS) balun amplifier with the S2D conversion [Fig. 3(a)]. The cross-coupled transistors Mn5A-B could calibrate the differential current imbalance and boost the gain as well as noise performance. Besides, an auxiliary Gm cell is introduced to break the design compromise among input matching, noise and gain performance. With the auxiliary Gm, the input impedance R_{in} and gain of the LNA are given by:

$$R_{in} = 1/(g_m + g_{mx}) \qquad Gain = 2(g_m + g_{mx})R_L \tag{1}$$

Here, R_L is the LNA load resistance. Hence, the LNA input impedance R_{in} is not only dependent on g_m provided by Mn1 but also dependent on g_{mx} provided by the Gm cell, which allows more degrees of freedom for optimal design. The gate bias of Mn1 is kept the same as Mn2-3 by a common-mode feedback loop in the auxiliary Gm to maintain constant LNA performance over the PVT variations. Since the loop gain G_{C_loop} has far less bandwidth than the desired RF frequency, this common-mode feedback loop has little effects on the LNA noise and gain performance. The role of the auxiliary Gm cell could be thought to increase the trans-conductance of both Mn1 and Mn2 without increasing the current consumption in proportion. In this work, the larger g_m and g_{mx} with the restriction of (g_m+g_{mx}) <38mS are adopted to achieve better noise performance while maintaining the input impedance matching S11<-10dB over the Sub-GHz band.

Since the Sub-GHz balun-LNA is wideband and provides limited attenuation to the 3rd-order harmonics, a harmonic-rejection RFA is cascaded to improve the HRR3 performance [Fig. 3(b)].

In the design, in order to attenuate the interference of -40dBm down to the noise floor, e.g. -102dBm in 10MHz BW mode with *NF*=5dB, an HRR3 of >62dBc is required. This attenuation is contributed by four parts, including the 1st-order low-pass filtering characteristic of the LNA (9dB), the notch filtering effect of the RFA, the load effect of the 4-path filter and the passive voltage mixer inherent rejection (9dB). The load effect of the passive voltage mixer driven by 25% duty-cycle LOs would introduce 19dB OB attenuation in theory [30]:

$$HRR3 = 9\sin^2(\frac{\pi}{4}) / \sin^2(\frac{3\pi}{4}) \tag{2}$$

However, as shown in Fig. 4, the simulated RFA normalized frequency response with the notch filter off exhibits only 14dBc HRR3 due to the mixer switch-on resistance, the limited RFA output impedance and parasitic capacitance. The notch filter in the RFA exhibits low impendence at the desired frequency and high impendence at the 3rd-order harmonics to improve the HRR3:

$$f_{pass@LO} = \frac{1}{2\pi\sqrt{L(C_1 + C_2)}} \qquad f_{notch@3*LO} = \frac{1}{2\pi\sqrt{LC_1}} \tag{3}$$

Thus, the RFA output HRR3 benefiting from the notch filtering can be expressed as:

$$\begin{aligned} HRR3(RFA) &= \frac{(g_{mn} + g_{mp})R_L(\omega)}{[1 + (g_{mn} + g_{mp})R_S(\omega)]} \cdot \frac{[1 + (g_{mn} + g_{mp})R_S(3\omega)]}{(g_{mn} + g_{mp})R_L(3\omega)} \\ &\approx 20\log_{10}[1 + (g_{mn} + g_{mp}) \cdot 3\omega \cdot L \cdot Q_{parallel}] + 14 \quad (dBc) \end{aligned} \tag{4}$$

where g_{mn} and g_{mp} are the trans-conductance of the current-reuse input transistors, R_L is the load of the RFA and R_S is the equivalent impedance of the notch filter. To achieve high HRR3, large L and Q are desired. In this work, a 4.8nH differential inductor with Q=12.5 and g_{mn}+g_{mp}≈18mS are chosen to trade-off between area overhead and power consumption. However, the obtained HRR3 is still limited to 51.2dBc, with the harmonic rejection provided by the LNA (9dB), the notch filter (19.2dB), the 4-path band-pass filter (14dB) and the mixer inherent rejection (9dB). In order to further improve the HRR3 performance, a current-reuse Q-enhanced circuit is introduced:

$$Q_{enh} = \frac{Q}{(g_{mn_{enh}} + g_{mp_{enh}})\omega LQ - 1} \tag{5}$$

Based on (4), Q_{enh} should be >48 to achieve 62dBc HRR3. However, Q_{enh} cannot be too high to avoid the linearity and noise degradation as well as self-oscillation issue. Thus, a programmable

current source is used to control Q_{enh}. Besides, two binary-weighted switched capacitor arrays (C_1 and C_2) are employed to tune the notch filter to cover the Sub-GHz band.

As shown in Fig. 5(a), a single-ended inductively source-degenerated LNA loaded by an LC tuned tank interfaces with the antenna in 2.4GHz band and provides some attenuation to the OB interferences. The LNA could also be configured into low gain mode when the peak detector based RF-AGC detects strong signals. Due to the limited quality factor of the on-chip inductor, the OB attenuation provided by the LNA is only effective for the blockers locating at >100MHz offset from the operation frequency. Then, a current-reuse active balun is inserted to convert the RF signals into the differential, as shown in Fig. 5(b). Compared with the traditional baluns, the poor common-mode noise rejection and second-order distortion suppression due to gain/phase imbalance are calibrated with two feedback loops, *Loop1* and *Loop2*. The complementary transistors M1A-D act as the input trans-conductance stage, and convert the single-ended input voltage into the imbalanced currents which are delivered to the compensation feedback loops. The differential output of the balun can be derived from the equivalent circuits in Fig.5(c) as follows:

$$\begin{aligned} V_{outn} &= \frac{1}{[(\frac{1}{R_L^{/}}+\beta_{loop1})^2-\beta_{loop2}{}^2]}[(\frac{1}{R_L^{/}}+\beta_{loop1})I_{in}-\beta_{loop2}I_{ip}] \\ V_{outp} &= \frac{-1}{[(\frac{1}{R_L^{/}}+\beta_{loop1})^2-\beta_{loop2}{}^2]}[\beta_{loop2}I_{in}-(\frac{1}{R_L^{/}}+\beta_{loop1})I_{ip}] \end{aligned} \tag{6}$$

Here, $R^{/}_L$ is the parallel resistance of the load R_L and the input impedance of the passive voltage mixer. Thus, the RFA is co-designed with the mixer. β_{loop1} and β_{loop2} are the feedback coefficients of two loops and can be independently adjusted by reconfiguring the bleeding currents to maintain constant performance over the PVT variations and various gain settings. Therefore, no matter how the gain and phase imbalances interact, *V(OP)* and *V(ON)* would be fully differential when equation (7) holds. In the design, to avoid the possible oscillation, a smaller β_{loop2} is chosen.

$$\frac{1}{R_L^{/}}+\beta_{Loop1}=\beta_{Loop2} \tag{7}$$

2) Reconfigurable Analog Baseband

Fig. 6 shows the schematic of the current-domain I/Q imbalance calibration, which is placed ahead of the channel filter to form a capacitive load for the passive voltage mixers. The imbalanced I/Q signals are converted into the current signals by both TCAs in the main and cross-coupled paths, and the following TILPF combines these current signals to obtain the calibrated I/Q signals. By configuring the trans-conductance of the TCAs in the main and the cross-coupled paths, the I/Q imbalance could be corrected. With $gm_i=gm_q=gm$, $\Delta gm_i=\Delta gm_q=\Delta gm$, $gm_{i->q}=gm_{q->i}=gm_{cross}$ and $\alpha=\Delta gm/gm$, $\theta=gm_{cross}/gm$, the calibrated I/Q signals can be derived as (high-order errors are ignored):

$$\begin{bmatrix} I_{cal} \\ Q_{cal} \end{bmatrix} = \begin{bmatrix} gm_i - \Delta gm_i & gm_{i->q} \\ gm_{q->i} & gm_q + \Delta gm_q \end{bmatrix} \begin{bmatrix} I_{imb} \\ Q_{imb} \end{bmatrix} = gm \cdot \begin{bmatrix} 1-\alpha^2-\theta^2 & 0 \\ 0 & 1-\alpha^2-\theta^2 \end{bmatrix} \begin{bmatrix} I_{Ideal} \\ Q_{Ideal} \end{bmatrix} \approx gm \cdot \begin{bmatrix} I_{Ideal} \\ Q_{Ideal} \end{bmatrix} \quad (8)$$

where 2α and 2θ are the differential gain/phase imbalance. With gm=1.55mS, Δgm=40uS and gm_{cross} =40uS, this I/Q imbalance calibration circuit is able to handle ±3dB gain error with 0.2dB/step and ±10.5° phase mismatch with 1.5°/step, thus the minimum 41.2dBc IRR can be achieved in theory. In most cases, the remaining gain error would be smaller than 0.2dB and phase mismatch is smaller than 1.5 ° after the calibration, so the achieved IRR would be higher than 41.2dBc. Besides, the capacitors before the TILPF help to further attenuate the OB interferences, and the TILPF output is connected to the peak detector based RF-AGC to detect the blocker signal strength.

The channel-select filter is a 1st/2nd/3rd-order reconfigurable Butterworth structure, and supports the complex band-pass mode (CBPF) with 1MHz/2MHz signal bandwidth or the low-pass mode (LPF) with 10MHz signal bandwidth to satisfy different channel selectivity and OB suppression requirements (Fig. 7). In order to save the power in different operation modes, the power-scalable technique with flexible op-amp array (FLOA) is employed, which consists of multiple op-amp cells and can adapt the GBW to the desired bandwidth by switching on/off each op-amp cell. As shown in Fig. 7, the op-amp cell adopts the dual-gain path and "anti-pole-splitting" techniques to enhance the GBW and save the power while maintaining high DC gain. The Class-AB output stage obtains

double gm and large output voltage swing. The high-speed path dominants at high frequency which helps to extend the GBW and improve the phase margin [31]. Moreover, the C_F with R_F forms an "anti-pole-splitting" action that moves the dominant pole to a higher frequency and extends the bandwidth. The reconfigurable filter consumes 0.64-3.84mW power in different operation modes.

Since the peak detector is unsuitable to indicate the received signal strength in OFDM systems, an accuracy-enhanced differential RSSI-based hybrid AGC with 50dB dynamic range is proposed (Fig. 8). The signal is firstly amplified by the three-stage PGA which is cascaded by the RSSI to sense the signal strength and output a DC voltage, then the following SAR ADC converts it to the digital domain and the digital logic generates the gain control codes for the PGA until the output power level meets the system requirements. Compared with the single-ended one [32], a differential RSSI is proposed to detect the input signal strength, which achieves better common-mode noise rejection and is more immune to the PVT variations. Moreover, since the conventional RSSI suffers from insufficient conversion accuracy with only one curve to cover the input signal strength range, a piecewise RSSI is adopted to divide the input signal strength range into three segments with bypass switches *SW1* and *SW2*. In SAR ADC, a new multi-phase clock generator based on the gate-controlled ring oscillator (GCRO) is proposed, which avoids the high-speed bit-by-bit feedback operation from SA logic to the clock generator.

B. Transmitter

1) Passive Voltage Modulators

In the transmitter, the output out-of-band noise is mainly from the mixer and analog baseband. The baseband noise can be partially filtered out by the passive filter before the mixer, so the noise from the mixer is more important. Since the traditional Gilbert mixer has poor noise and linearity performance, in order to achieve the low OB noise and better linearity, large power consumption is required. Recently, many efforts have aimed to combine the mixer and the power amplifier into a power mixer to improve the efficiency [33]-[34]; however, it needs another current conversion circuit. In this work, the passive voltage modulator is employed to achieve low OB noise and save

the power. Moreover, unlike the RX, the gain of the mixer seems less important than the linearity and the small gain of the passive mixer could be easily compensated by the analog baseband.

Ideally, the passive voltage mixer driven by 50% duty-cycle LOs has 3dB higher conversion gain than the one driven by 25% duty-cycle LOs, which can be explained as:

$$F_{25\%}(t)=\frac{\sqrt{2}}{\pi}[cos\omega_{LO}(t)+\frac{1}{3}cos3\omega_{LO}(t)+\cdots] \qquad F_{50\%}(t)=\frac{2}{\pi}[cos\omega_{LO}(t)+\frac{1}{3}cos3\omega_{LO}(t)+\cdots] \tag{9}$$

However, due to the overlap of the 50% duty-cycle LOs, the baseband voltage would be halved at the mixer input, as shown in Fig. 9. Thus, the passive voltage mixer driven by 50% duty-cycle LOs offers 3dB lower gain than the one driven by 25% duty-cycle LOs. In order to save the power, passive voltage mixers driven by 25% and 50% duty-cycle LOs are employed in the dual bands, respectively. In Sub-GHz band, the mixer equivalent input impedance can be given by [35]:

$$Z_{mix}=R_{SW}+\frac{1}{2f_{LO}C_{Load}} \tag{10}$$

where C_{Load} is the single-ended input capacitance of the PA driver and R_{sw} is the switched-on-resistance. It indicates that the analog baseband is loaded by a small impedance due to the LO switch effect. Especially in 2.4GHz band, the equivalent input impedance Z_{mix} of the mixer driven by 50% duty-cycle LOs would decrease more sharply compared with the mixer driven by 25% duty-cycle LOs. In this work, the passive LPF is flexibly reconfigurable (R_1 from *14.25Ω to 114Ω* with 4 control bits, R_2 from *220Ω to 2.2KΩ* with 4 control bits and C_3 from *0.48pF to 4.8pF* with 3 control bits) to maintain the same gain and bandwidth in the dual bands, and more current consumption is needed to enhance the TILPF driving capability for 2.4GHz band.

2) Dual-Band PAPR-Tolerant PAs

As illustrated in Table I, the efficiency of a linear PA decreases sharply at the back-off powers. However, if the optimal load is increased by $\times 1/p^2$ (here p represents the scaling factor, and $p<1$) and the DC current is decreased by $\times p^2$, the drain efficiency would remain constant. Thus, the PA's efficiency at back-off powers can be improved by dynamically modulating the load and modifying the effective power cells [36]. In this work, the linear PAs with mode switching scheme are proposed to boost the back-off efficiency.

Assuming that the output impedance matching network is lossless, the conversion gain of the PA can be expressed as:

$$(g_m R_{opt} V_{in})^2 / (2R_{opt}) = V_{out}^2 / (2R_L) \quad \Rightarrow \quad CG = 20log(V_{out}/V_{in}) = 20log(g_m \sqrt{R_{opt} R_L}) \tag{11}$$

Here, g_m is the trans-conductance of the PA, R_{opt} is the optimal load and R_L is the output load (50Ω). When the PA operates at the 6dB back-off power, 3/4 of the power transistors would be powered off and the optimal load increases to $4R_{opt}$. Then, the updated conversion gain is given by:

$$CG_{-6dB} = 20log(\frac{1}{4} g_m \sqrt{4R_{opt} R_L}) = CG - 6 \tag{12}$$

Fortunately, this gain drop of the power stage can be compensated with the driver stage to achieve constant gain, and the slight increased power consumption of the driver stage due to gain compensation is negligible compared with the power saved from the load modulation. Furthermore, the discontinuities which just occur occasionally when the PAPR happens have litter impact on the average EVM while degenerate the peak EVM very much. Fig. 11(a) shows the simulated peak EVM performance verse phase and gain discontinuities, from which, the gain and phase discontinuities should be less than 0.5dB and 10.5° to achieve ≤-14dB peak EVM. The gain discontinuities could be measured by setting the PA operation modes manually, which shows less than 0.5dB gain variation during the modes switching, as discussed in Section IV.

Three issues exist to design such a PAPR-tolerant PA: (1) a load modulation network is needed to transform R_L to the optimal load R_{opt} at the back-off power; (2) gain and phase discontinuities due to the load modulation and driver stage compensation should be minimized; (3) a power-control loop is needed to dynamically reconfigure the PA operation modes to improve the average efficiency. Table II shows the PA operation modes in Sub-GHz and 2.4GHz bands, respectively.

In order to address the first issue, the design scheme with the fixed-inductor is explored since the switched-inductor scheme may occupy more area or have lower quality factor, compared with the switched-capacitor scheme. As a result, the capacitor-tapped and π-type matching networks are selected as the best candidates, as shown in Fig. 10, whose equivalent admittance Y_{IN} and loaded quality factor Q_{load} can be derived as:

$$Y_{IN\_T} = Y_{R\_T} + \frac{1}{j\omega L_T} + j\omega C_T = \frac{\omega^2 R_L C_1^2}{1+\omega^2 R_L^2 (C_1+C_2)^2} + [\frac{1}{j\omega L} + j\omega C_X + j\omega \cdot \frac{\omega^2 R_L^2 C_1 C_2 (C_1+C_2) + C_1}{1+\omega^2 R_L^2 (C_1+C_2)^2}] \quad (13)$$

$$Y_{IN\_PI} = Y_{R\_PI} + \frac{1}{j\omega L_{PI}} + j\omega C_{PI} = \frac{R_L}{\omega^2 L^2 + R_L^2 (1-\omega^2 LC_2)^2} + [\, j\omega (C_1 + C_X) - j\omega \cdot \frac{L - R_L^2 C_2 (1-\omega^2 LC_2)}{\omega^2 L^2 + R_L^2 (1-\omega^2 LC_2)^2}] \quad (14)$$

$$Q_{load\_T} = \frac{\omega C_T}{Y_{R\_T}} = \frac{1}{\omega L_T Y_{R\_T}} \qquad Q_{load\_PI} = \frac{\omega C_{PI}}{Y_{R\_PI}} = \frac{1}{\omega L_{PI} Y_{R\_PI}} \quad (15)$$

where (Y_{R_T}, L_T, C_T) and (Y_{R_PI}, L_{PI}, C_{PI}) are the equivalent parallel real admittance, inductance and capacitance of the two matching networks. Besides, the power loss in the matching network can be expressed as ($Q_{intrinsic}$ is the intrinsic quality factor of the passive components):

$$P_{loss} = P_{out} \cdot Q_{load} / Q_{intrinsic} \quad (16)$$

It indicates that for a given $Q_{intrinsic}$, the efficiency of the matching network increases as Q_{load} reduces. Fig. 11(b) plots the loaded quality factor Q_{load}, which shows that the capacitor-tapped matching network has a lower quality factor than the π-type one, thus resulting in higher power efficiency. In the design, the capacitor-tapped matching network is adopted and it only needs one differential inductor to save the area. Besides, its optimal load $1/Y_{R\_T}$ as expressed in (12) is only dependent on the ratio of C_1 and C_2, thus achieving good robustness to the PVT variations.

Since the gain discontinuity is compensated by the driver stage, the second issue mainly focuses on the phase discontinuity due to the abrupt phase change of the matching network during the mode switching, which can be explained as (16), mainly due to the Q_{load} change in different modes.

$$\theta_\omega = -arctan Q_{load} (\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}) \approx -arctan Q_{load} (\frac{2\Delta\omega}{\omega_0}) \quad (17)$$

Fig. 11(c) plots the Sub-GHz band PA phase discontinuity in three modes HPM/MPM/LPM versus different inductance, which shows that the phase discontinuity reduces with the larger inductance. In the design, a 9.6nH differential inductor with $Q_{intrinsic}$=12.2 is used to trade-off among area overhead, power loss and phase discontinuity issue. As shown in Fig. 12, the single-ended optimal load of Sub-GHz PA calculated from the load-pull simulations is Y_{opt}=(1/100-j*1/137)S in HPM, (1/176-j*1/200)S in MPM and (1/470-j*1/4425)S in LPM. The 2.4GHz PA is designed in the similar way, which adopts a 5.1nH differential inductor with $Q_{intrinsic}$=13.8.

The Sub-GHz PA has three operation modes: low power mode (LPM), middle power mode (MPM) and high power mode (HPM). As shown in Fig. 13, it consists of three parallel branches (each branch consists of a driver stage and a power stage to reduce the load effects of the driver stage in different modes) and a shared dynamic load modulation network. Since the power loss caused by the output matching network increases as the optimal load increases, three branches are implemented with the proportion of 1:2:2 rather than the theoretical 1:3:4. In LPM, only the top branch is powered on and the optimal load is configured to a large value; in MPM, the upper two branches are activated and the optimal load is set to a middle value; while in HPM, all the branches are enabled and the optimal load is the smallest to achieve the highest output power.

The 2.4GHz PA has two operation modes: low power mode (LPM) and high power mode (HPM). Similarly, it is composed of two parallel branches and a shared dynamic load modulation network (Fig. 14). However, the driver stages of the two branches share the same LC tuned load to save the area. In LPM, only the upper branch is powered on and the optimal load is configured to a large value; in HPM, both two branches are enabled with the smallest optimal load. Moreover, the PA power stages in each band have three parallel sub-branches which are divided into 1:1:2 to offer programmable gain, increase the dynamic range of the transmitter by 12dB (4 steps with -12,-6,-2.5 and 0dB normalized gain) and reduce the power consumption as the average output power decreases in each operation modes.

To cope with the third issue, a mixed-signal power-control loop is proposed to dynamically reconfigure the PA's operation modes, as shown in Fig. 15. First, the power detector monitors the instantaneous input signal PAPR and transfers the message to the following comparator array; then, the digital power-control block, which decodes the outputs from the comparator array and generates the configuration codes for the PA parallel branches and the capacitor bank in the matching network, is employed to control the PA operation mode (the driver stage, power stage and load modulation matching network). In the design, the replica technique is employed in the power detector to maintain the output DC voltage constant over the PVT variations and avoid the

misjudgment. The thresholds for the comparator array are also designed reconfigurable for efficiency optimization for a fixed PARP. Fig. 16 shows the PA automatic mode switching process, exhibiting that the PA output waveform well follows the input signal with the help of the proposed power-control loop.

Furthermore, some techniques have been implemented to reduce the crosstalk between the PA and the VCO. Firstly, the VCO and the PA are powered by separate power supplies to avoid the crosstalk through the supply. Secondly, in the layout, the frequency synthesizer has been surrounded by three guard rings with NTN layer, substrate contact, deep N-well, then substrate contact, to increase the isolation and reduce the crosstalk through the substrate. Thirdly, the electromagnetic simulation has been utilized to optimize the floor-plan of the VCO and the PA and reduce the coupling through the inductors in the VCO and the PA. Fourthly, the PA is grounded by 6 ground pads. Finally, the VCO is oscillating at 2x frequency of the PA, which mitigates the crosstalk a lot.

C. Frequency Synthesizer

A Σ-Δ fractional-N frequency synthesizer is integrated in this transceiver, with frequency coverage of 0.73-1.03GHz in Sub-GHz band and 2.21-2.60GHz in 2.4GHz band, and a frequency resolution of <30Hz. As shown in Fig. 17, the frequency synthesizer consists of two switchable Class-C VCOs, a CML-type divided-by-2 divider for Sub-GHz band and another two divided-by-2 dividers cascaded to form the divided-by-4 divider for 2.4GHz band, and a shared phase-frequency detector, a charge pump with 320uA output current, an off-chip 3rd-order loop filter and a Σ-Δ modulator to provide a fractional division ratio. In order to provide 4-phase LO signals for the quadrature mixers, the VCO works at twice the LO frequency and then divided by 2.

IV. MEASURED RESULTS

The proposed transceiver has been implemented in 180nm CMOS and occupies an area of 4.5×3.5mm^2 including ESD/IOs and pads, as shown in Fig. 18.

Fig. 19(a) shows the RF filtering characteristics of the Sub-GHz receiver with 5MHz single-side

bandwidth (10MHz BW), which improves the OB attenuation by 12dB at 20MHz offset. Fig. 19(b) shows the measured results in three operation modes with RF filtering off, in which the low-pass single-side bandwidth is 5MHz, and the complex band-pass bandwidth is 1MHz and 2MHz with 3MHz IF. Fig. 20(a) shows the measured 3rd-order harmonic rejection performance in Sub-GHz band, exhibiting average 60dBc HRR3 when all the negative resistance generators are powered on. Compared with the powered-off cases, 11dB improvement has been achieved. Fig. 20(b) shows the receiver image rejection ratio (IRR) in the low-IF mode after the I/Q imbalance calibration.

Fig. 21(a) shows the RSSI output voltage versus output power, which adopts three segments with each covering 20dB dynamic range. This RSSI is capable of indicating -50~+10dBm output power range with the effective conversion voltage from 0.3V to 1.4V and the maximum 2dBm linearity error. The measured PGA dynamic range and gain step are plotted in Fig. 21(b), demonstrating 0.2~48.6dB gain range with ~1dB/step. As shown in Fig. 22(a), the ADC achieves the SNR of 54.6dB with ~9bits effective resolution. The measured AGC locking process is shown in Fig. 22(b). With the RF input signal strength varying from -75dBm to -67dBm and AGC turned on, the PGA output waveform can be locked within 10us.

The receiver noise figure is measured by injecting a single-tone -87dBm RF signal into the LNA input, recording the ADC outputs with a FPGA and then performing the FFT on a PC. Fig. 23 shows the measured results in the dual bands. According to "$NF= 174-10\times log(BW)-SNR_{out}+P_{RF}$", the receiver obtains an equivalent *NF* of 5.1dB and 4.2dB for Sub-GHz and 2.4GHz bands, respectively.

The phase noise (PN) of the frequency synthesizer is plotted in Fig. 24 (a), showing -121dBc/Hz PN at 1MHz offset. Moreover, when compared with the Class-A operation, up to 5dB PN improvement is achieved by using Class-C VCO under the same current consumption. Similar measured results for the 2.4GHz band have been shown in Fig.24 (b).

Fig. 25(a) shows the PA PAE versus the output power in both bands. In Sub-GHz band, 16.3dBm OP1dB with 25% PAE is achieved in HPM, and the PAE is improved by ×3.24 (up to 16.5%) and ×1.41 (up to 20.9%) at 9dB and 3dB back-off powers (normal power back off level depends on the

modulation signal PAPR), respectively. In 2.4GHz band, an OP1dB of 14.8dBm with 25% PAE is obtained in HPM and the PAE is improved by ×2.17 (up to 15.8%) at 6dB back-off power. Fig. 25(b) shows the power detector output voltage versus input power in Sub-GHz band, exhibiting sufficient sensitivity for the power-control loop to judge the input PAPR and reconfigure the PA's operation modes.

Fig. 26 shows the power gain of the dual-band PAs over different operation modes. After configuring the gain of the driver stage, the Sub-GHz band PA has achieved a power gain of about 22.5dB with <0.5dB variation among the proposed three operation modes. Similar measurements to the 2.4GHz band PA show that 20.5dB power gain with <0.5dB variation between HPM and LPM has been achieved.

Finally, in order to verify the whole transmitter performance and for convenience to compare with other works, system modulation experiments are performed with 10MHz LTE signals. As shown in Fig. 27, the 850MHz LTE 16QAM signal with 5.0dB-PAPR is evaluated through the transmitter in Sub-GHz band, which exhibits the ACLR1/2 of -35.0/-51.5dBc and an EVM of 3.7% at 12.9dBm average output power. In 2.4GHz band, the ACLR1/2 of -34.2/-50.8dBc and an EVM of 3.9% is achieved at 10dBm average output power with 2.45GHz LTE 16QAM signals with about 5dB PAPR. Table III summarizes the transceiver performance and makes a comparison with the state-of-the-art.

V. CONCLUSIONS

This paper presents a fully-integrated reconfigurable dual-band transceiver for short range wireless communications. In Sub-GHz band, a Q-enhanced notch filtering RFA is introduced to achieve the maximum 75dBc HRR3. In 2.4GHz band, a single-ended-to-differential RFA with gain/phase imbalance compensation is proposed. Class-C VCOs are employed in the Σ-Δ fractional-N PLL frequency synthesizer to save the power. Moreover, multi-mode CMOS PAs with the proposed power-control loops are employed to enhance the back-off efficiency. Implemented in 180nm CMOS, this presented transceiver has achieved comparable or even better performance in terms of noise figure, HRR3, output power and power efficiency compared with other works.

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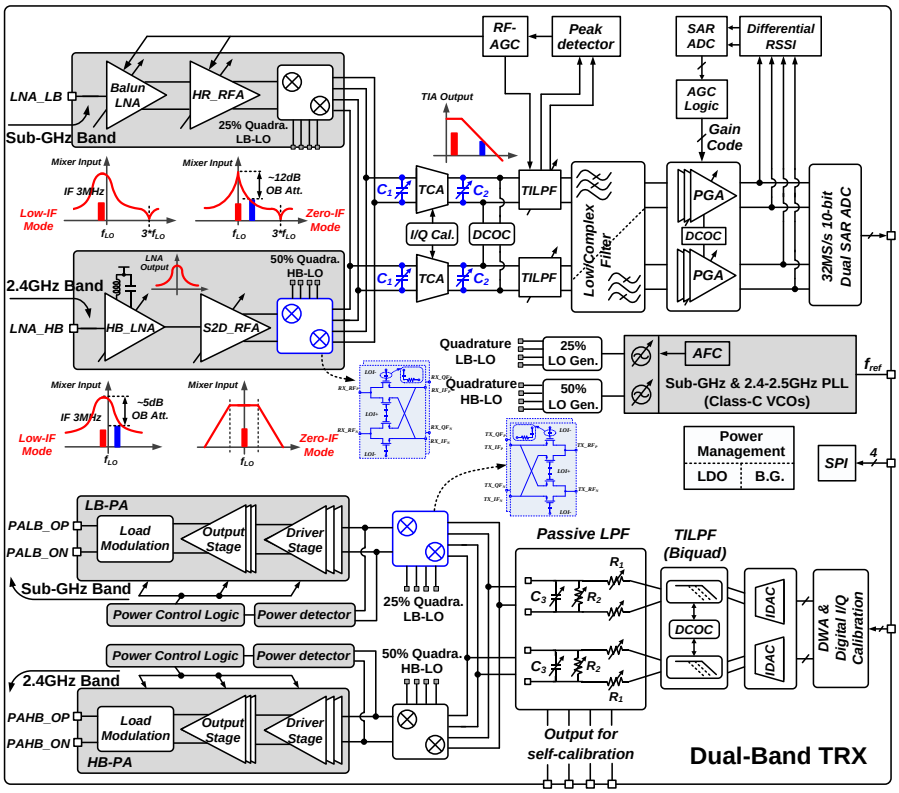

Fig. 1. Block diagram of the proposed reconfigurable dual-band transceiver.

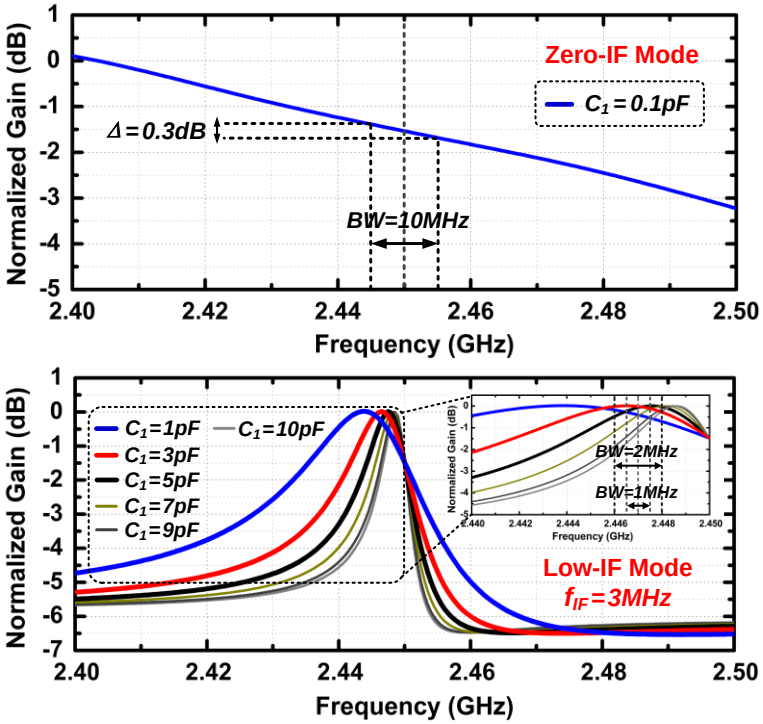

Fig. 2. Simulated filtering characteristics at the 50% duty-cycle clocking mixer input with different capacitance C_1 @ f_{LO}=2.45GHz.

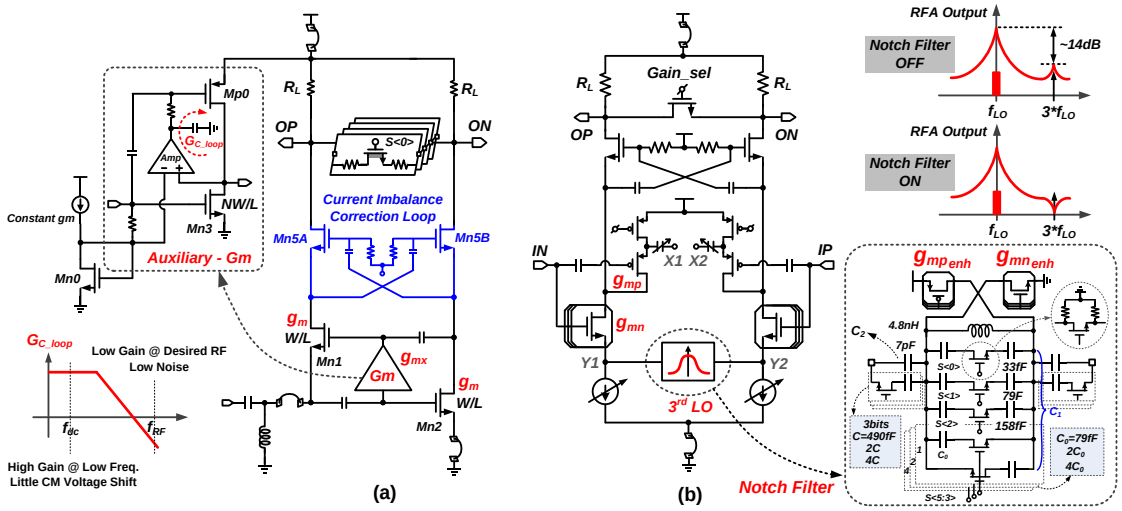

Fig. 3. The schematic of (a) Sub-GHz balun-LNA and (b) Sub-GHz harmonic-rejection RFA.

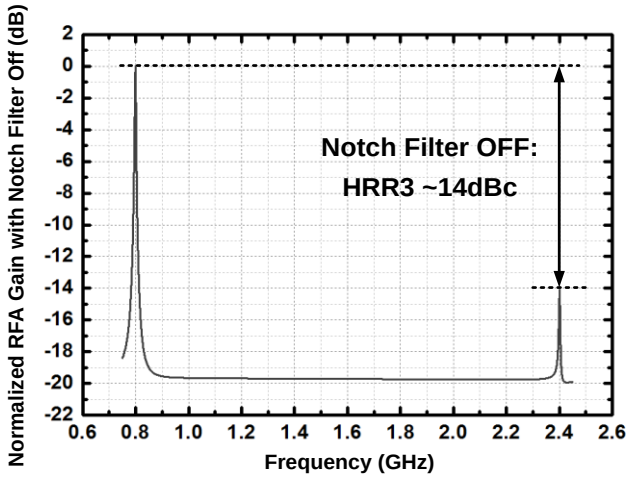

Fig. 4. Simulated RFA normalized frequency response with notch filter off.

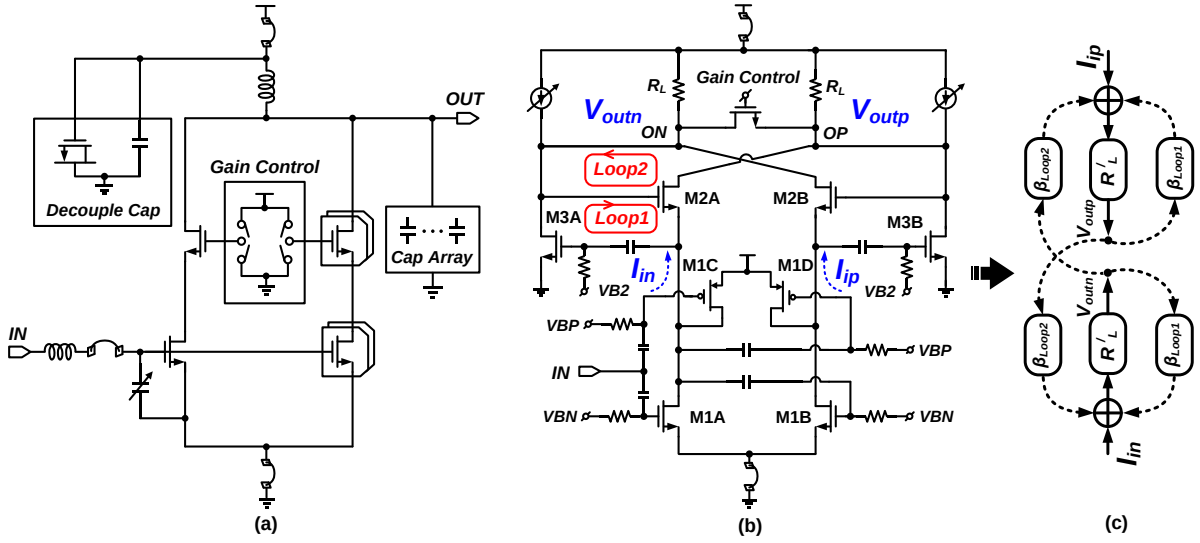

Fig. 5. The schematic of (a) 2.4GHz LNA, (b) 2.4GHz balun-RFA, (c) Balun equivalent circuit

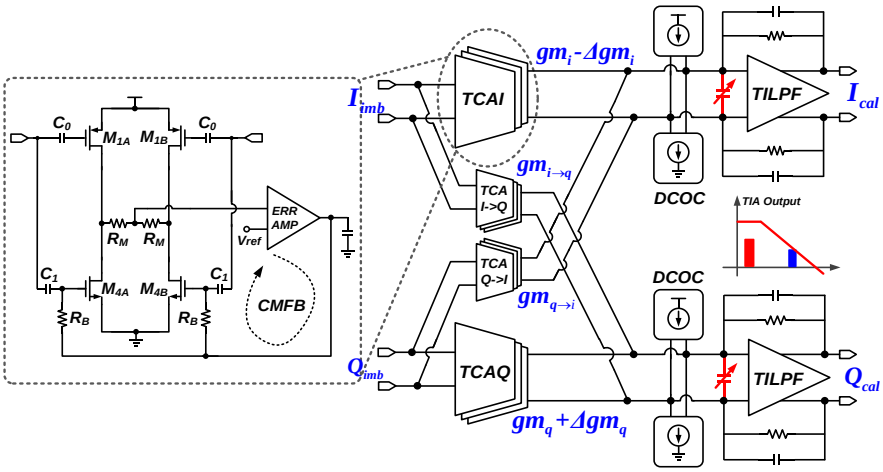

Fig. 6. Schematic of the current-domain I/Q imbalance calibration circuit.

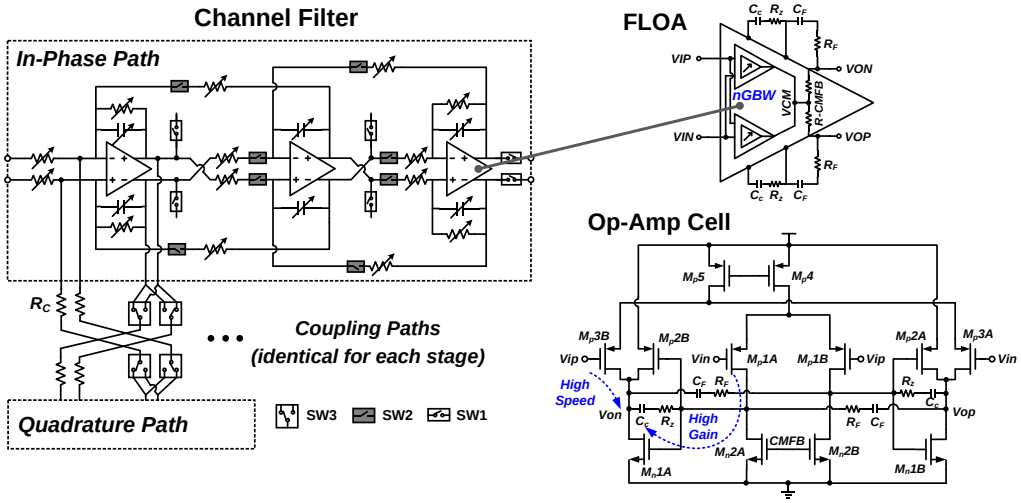

Fig. 7. Block diagram of the reconfigurable channel filter and the op-amp cell in the FLOA.

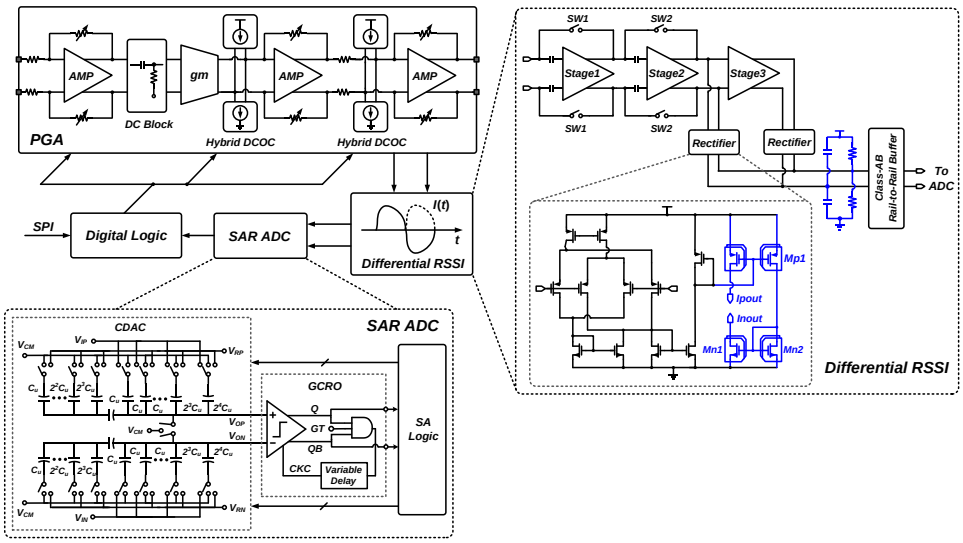

Fig. 8. Schematic of the differential RSSI-based hybrid AGC.

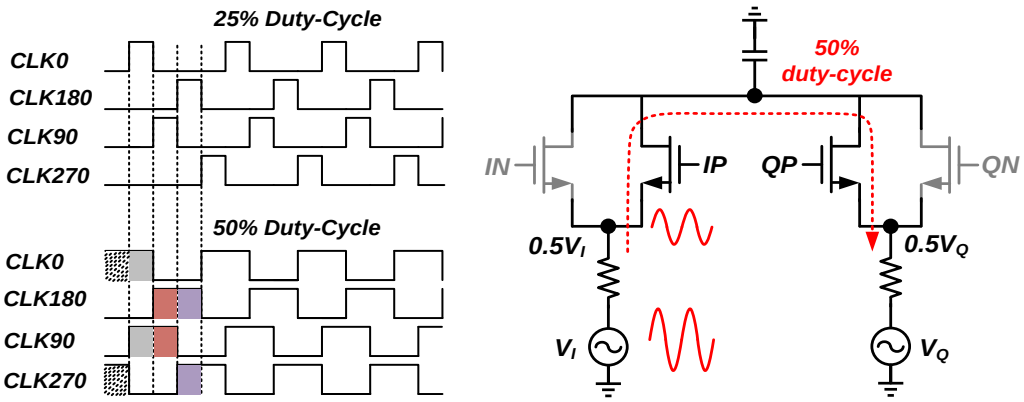

Fig. 9. Comparison of the passive voltage modulators driven by 25% and 50% duty-cycle LOs.

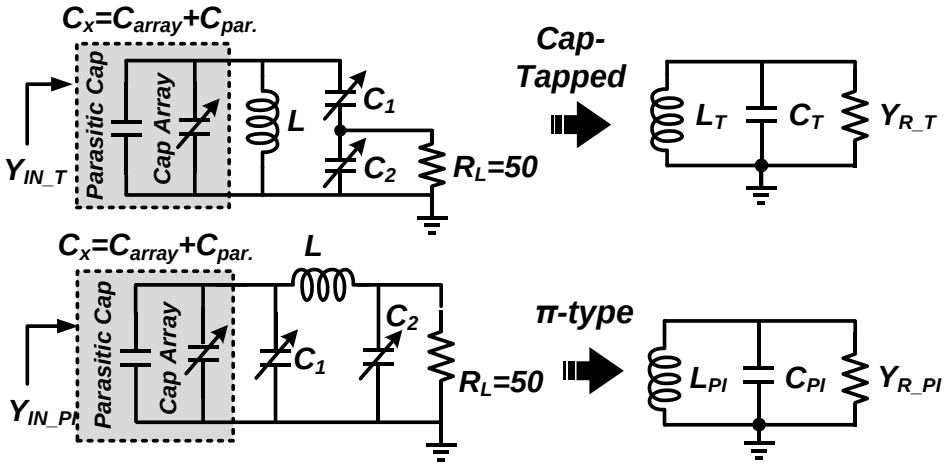

Fig. 10. The equivalent circuit of the capacitor-tapped and π-type matching networks.

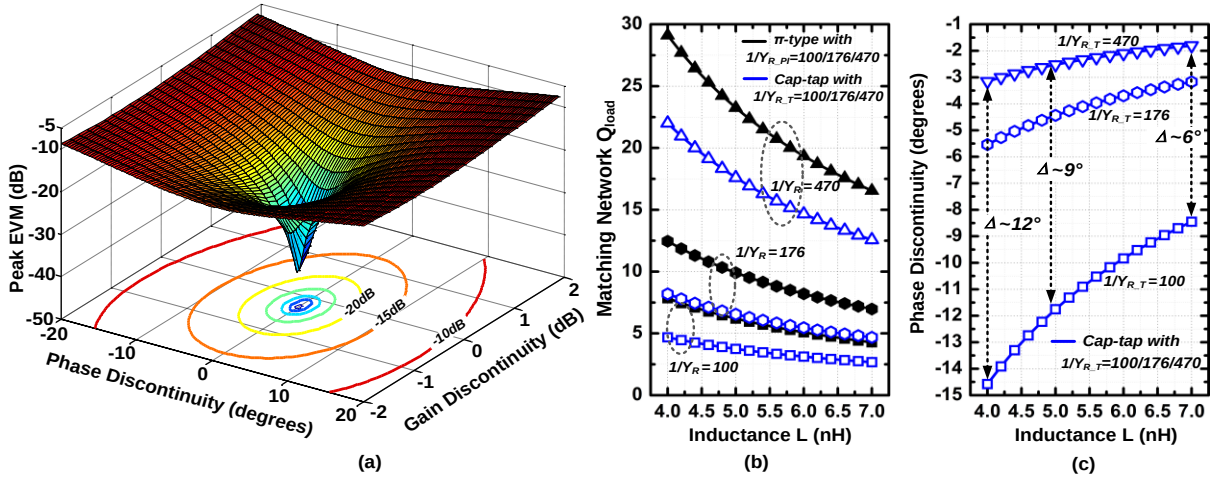

Fig. 11. (a) Simulated peak EVM versus the gain and phase discontinuities, (b)Simulated Q_{load} of the π-type and capacitor-tapped matching networks with different inductance, (c) Simulated PA phase discontinuities at 850MHz with different inductance.

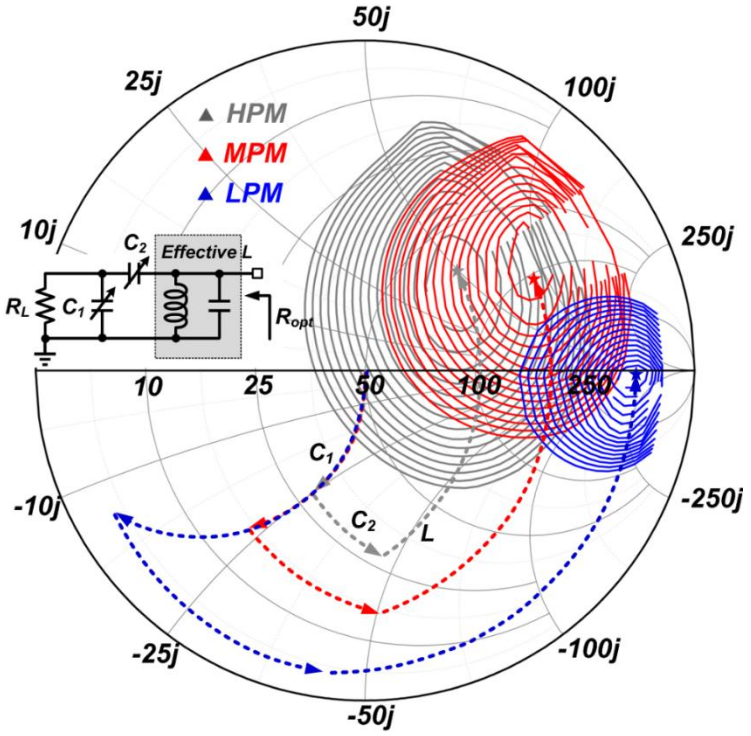

Fig. 12. Simulated load-pull contours of the Sub-GHz PA in HPM/MPM/LPM at 850MHz.

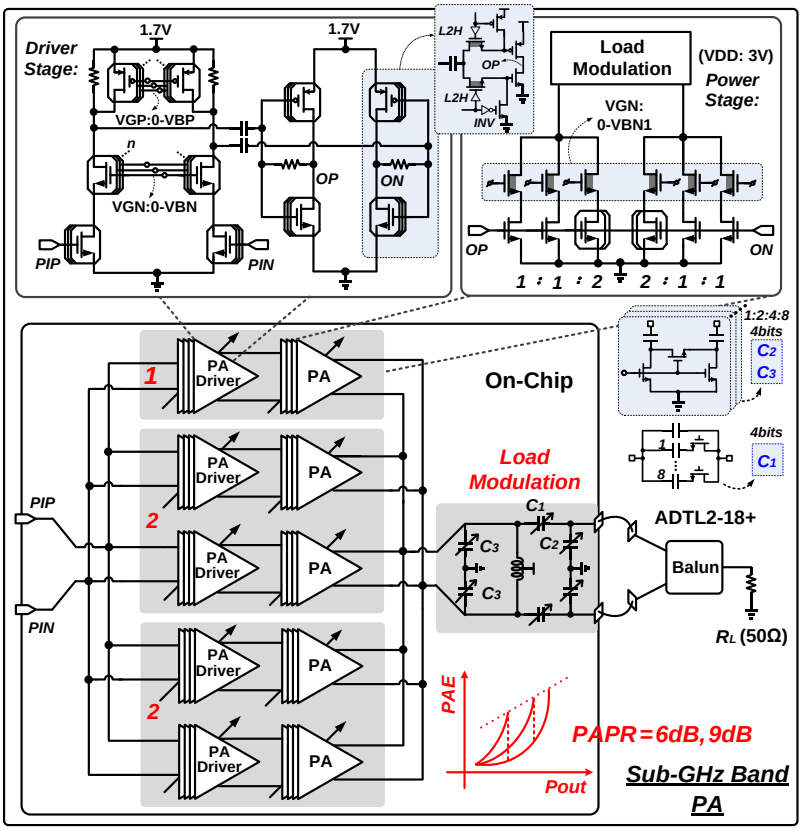

Fig. 13. The schematic of the Sub-GHz PA.

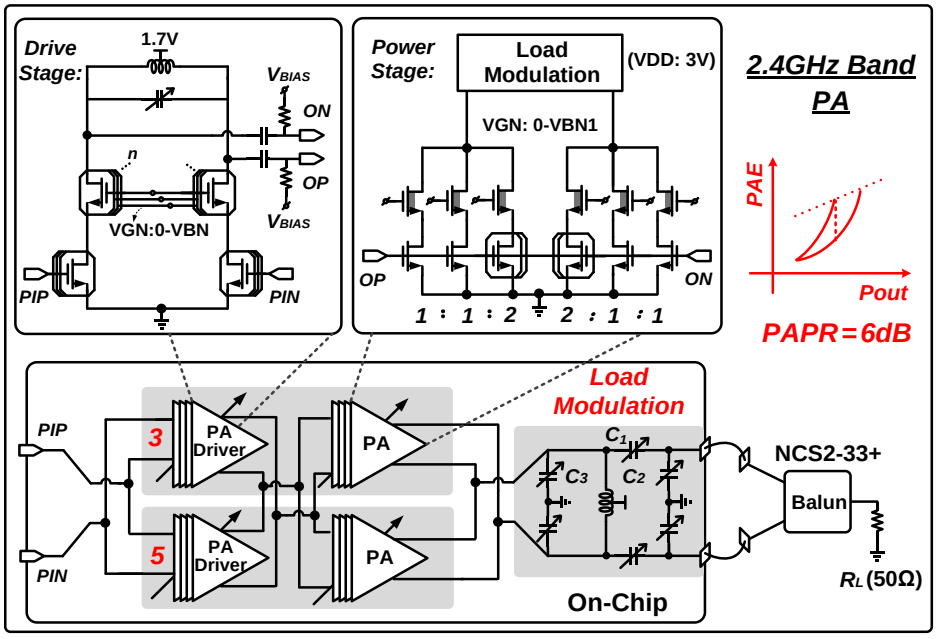

Fig. 14. The schematic of the 2.4GHz PA.

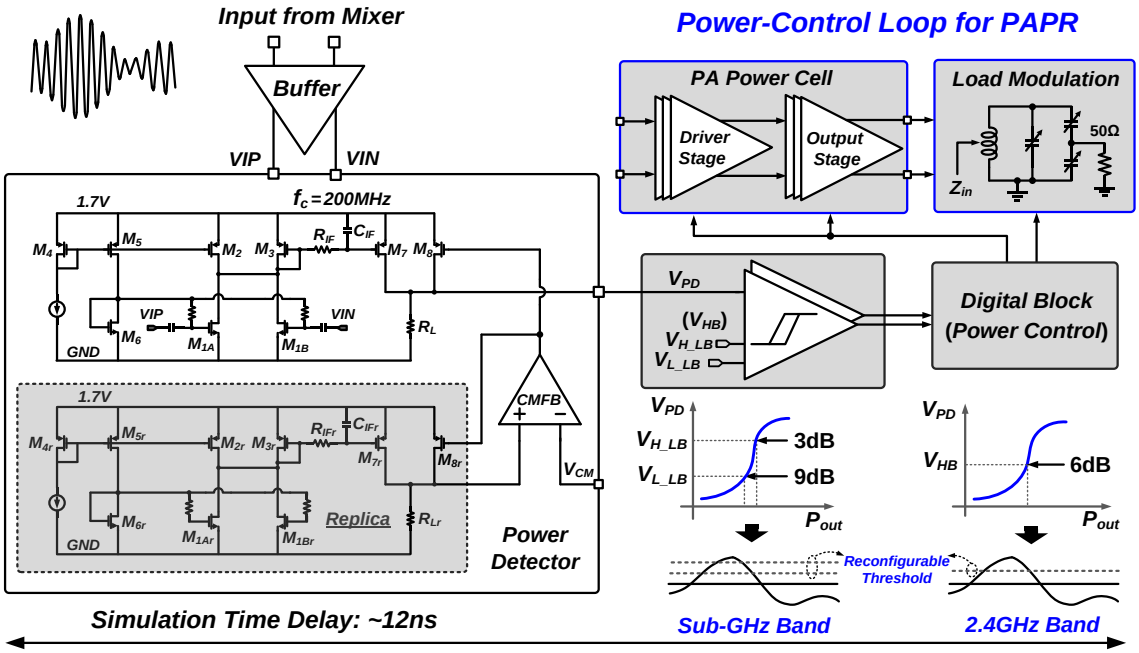

Fig. 15. Block diagram of the PA power-control loop for mode switching.

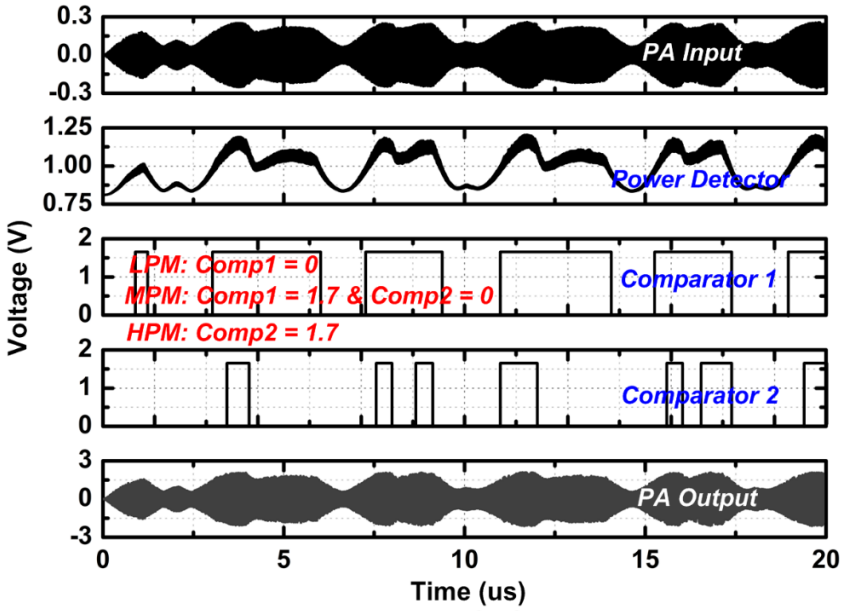

Fig. 16. Simulated waveforms of the Sub-GHz PA with the power-control loop.

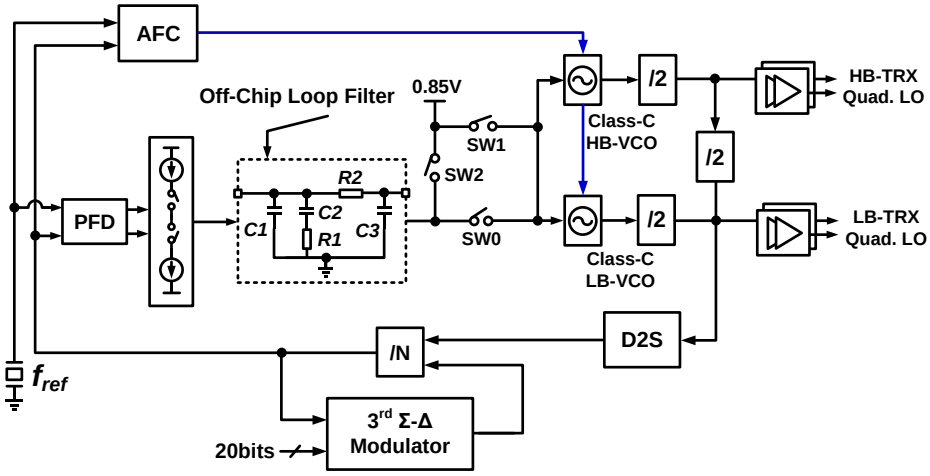

Fig. 17. Block diagram of the frequency synthesizer.

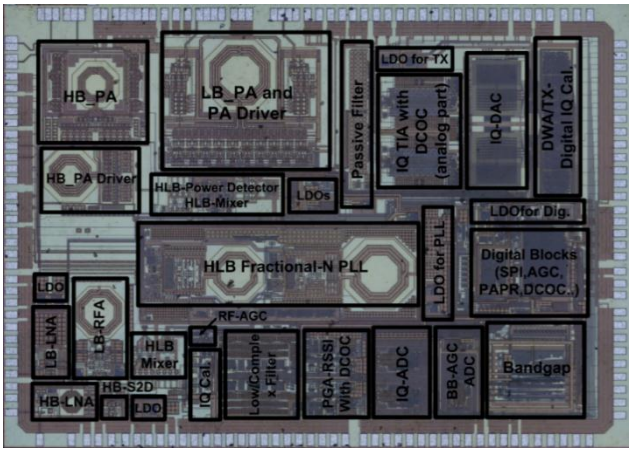

Fig. 18. Die microphotograph of the proposed dual-band transceiver.

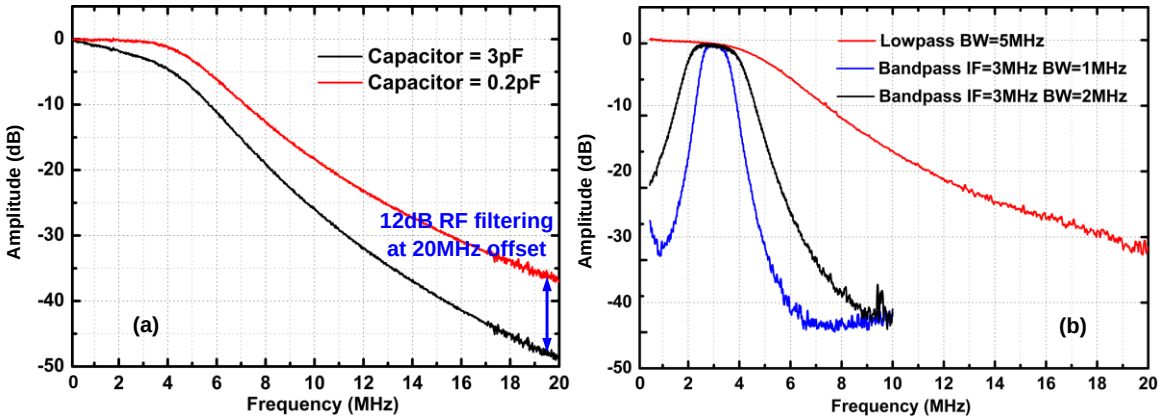

Fig. 19. (a) Measured RF filtering characteristics of the Sub-GHz receiver with 5MHz single-side analog baseband bandwidth. (b) Measured RX frequency response with RF filtering off.

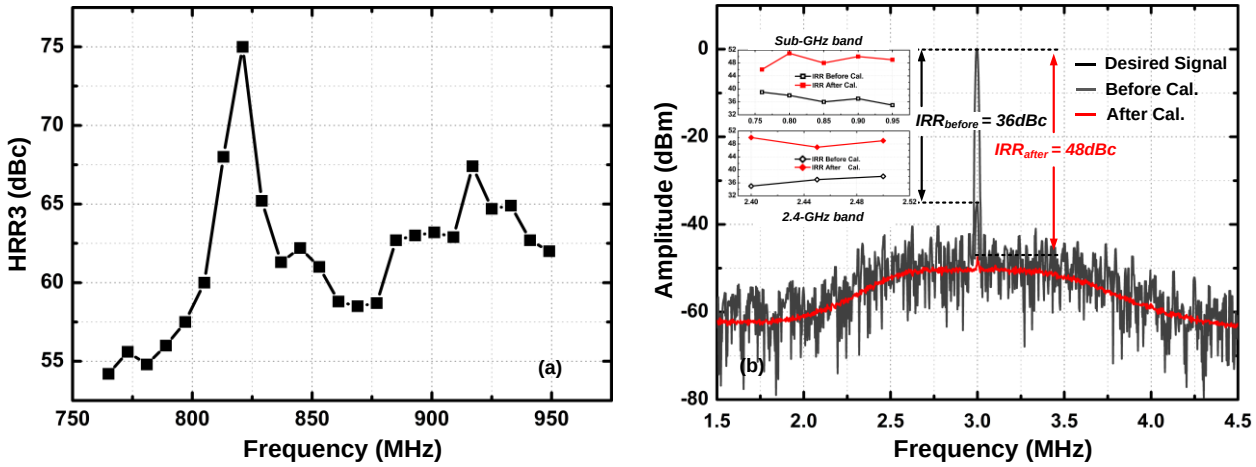

Fig. 20. Measured RX (a) HRR3 in Sub-GHz band and (b) IRR after I/Q calibration.

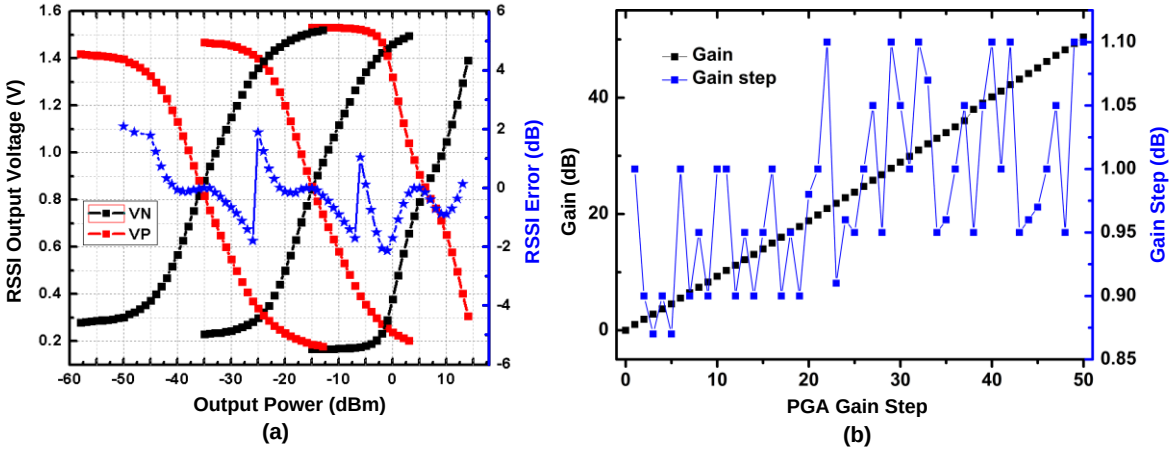

Fig. 21. Measured (a) RSSI output voltage versus output power and (b) PGA gain characteristics.

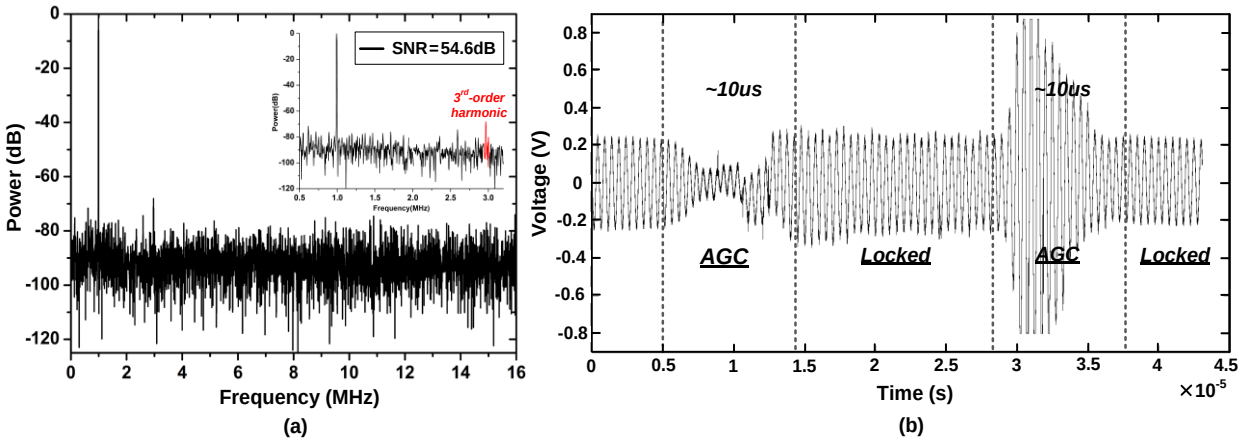

Fig. 22. Measured (a) ADC output spectrum and (b) AGC locking process.

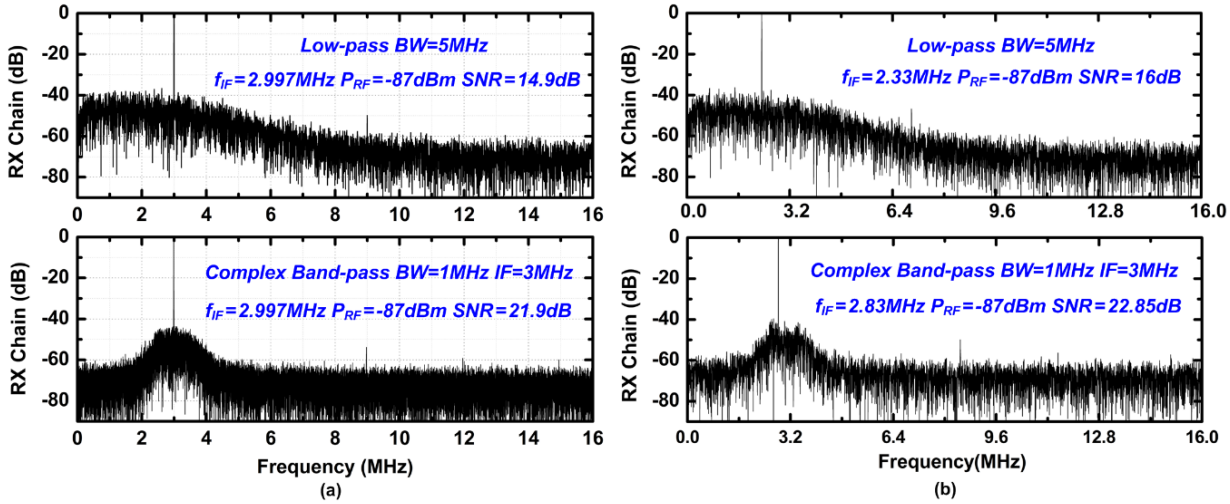

Fig. 23. Measured output FFT of the receiver chain in (a) Sub-GHz and (b) 2.4GHz bands.

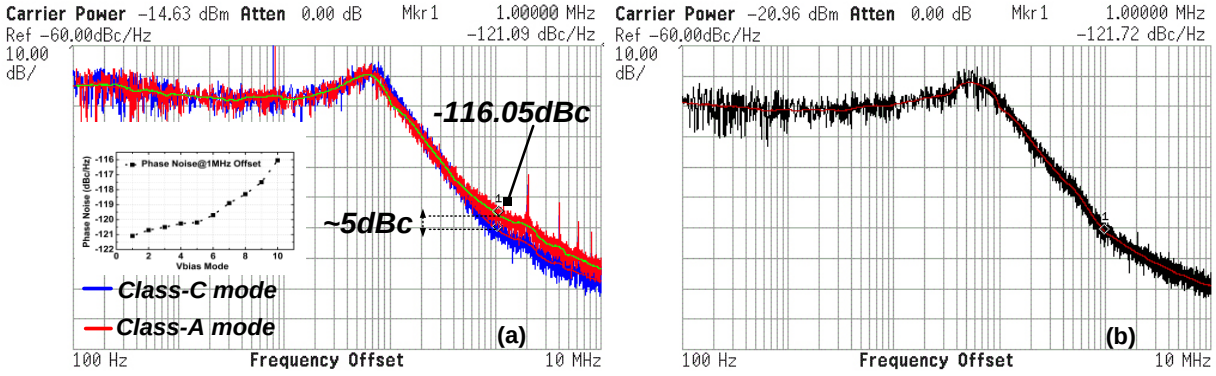

Fig. 24. Measured phase noise of the frequency synthesizer (a) Class-A/C mode comparison @1.7GHz carrier, (b) Class-C mode @4.864GHz.

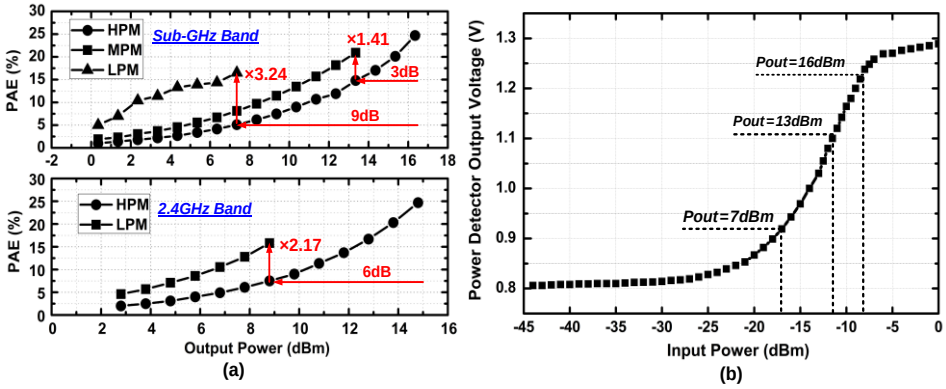

Fig. 25. (a) Measured PA PAE versus output power in Sub-GHz and 2.4GHz bands. (b) Measured power detector output voltage versus the input power for Sub-GHz band.

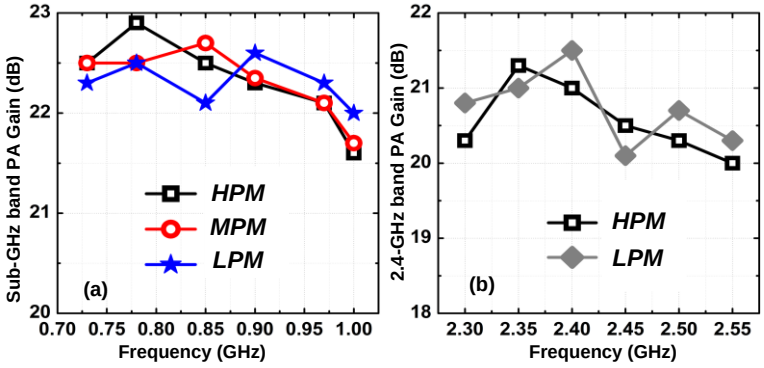

Fig. 26. Measured power gain of the dual-band PA (a) Sub-GHz band, (b) 2.4-GHz band

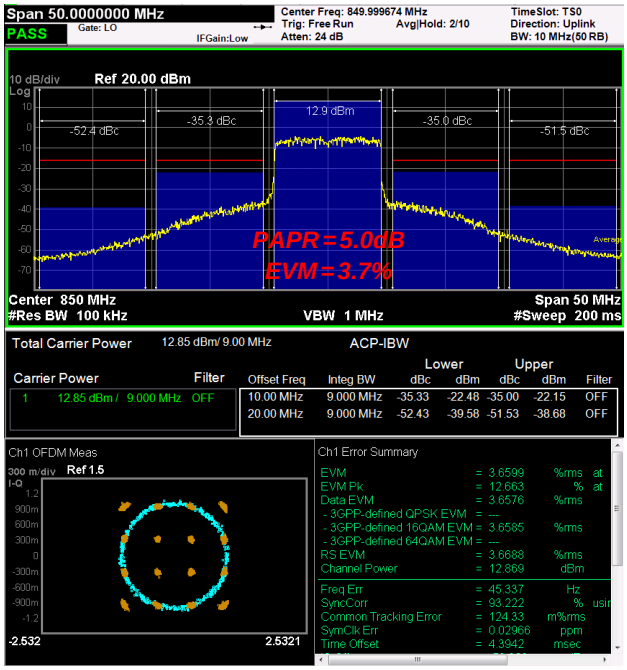

Fig. 27. Measured transmitter ACLR and constellations in 10MHz-LTE 16QAM @ f_{LO}= 850MHz with the PA closed-loop operation.

Table I A LINEAR PA EFFICIENCY VERSUS DIFFERENT INPUT SIGNAL STRENGTH

Method	**Fixed Load**	**Fixed Load**	**Variable Load**
Input signal	$\boldsymbol{V_{in}}$	$\boldsymbol{pV_{in}}$	$\boldsymbol{pV_{in}}$
Fundamental Current	$\boldsymbol{i_1}$	$\boldsymbol{pi_1}$	$\boldsymbol{p^2 i_1}$
Drain Voltage Swing	$\boldsymbol{v_1}$	$\boldsymbol{pv_1}$	$\boldsymbol{v_1}$
R_{opt}	$\boldsymbol{v_1/i_1}$	$\boldsymbol{v_1/i_1}$	$\boldsymbol{v_1/(p^2 i_1)}$
Output Power	$\boldsymbol{i_1 v_1/2}$	$\boldsymbol{p^2 i_1 v_1/2}$	$\boldsymbol{p^2 i_1 v_1/2}$
DC Power	$\boldsymbol{I_{DC} V_{DC}}$	$\boldsymbol{I_{DC} V_{DC}}$	$\boldsymbol{p^2 I_{DC} V_{DC}}$
Drain Efficiency	$\boldsymbol{i_1 v_1/(2 I_{DC} V_{DC})}$	$\boldsymbol{p^2 i_1 v_1/(2 I_{DC} V_{DC})}$	$\boldsymbol{i_1 v_1/(2 I_{DC} V_{DC})}$

Table II OPERATION MODES OF THE PAPR-TOLERANT PA IN SUB-GHZ AND 2.4GHZ BANDS

Band	Frequency (GHz)	PAPR (dB)	OP1dB (dBm)	Efficiency Enhancement
Sub-GHz	0.76-0.96	6/9	16.3/13.3/7.3	×1.41/ ×3.24
2.4GHz	2.4-2.5	6	14.8/8.8	×2.17

TABLE III PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART

Index	This work		Dual-band TRX				2.4GHz band		Sub-GHz band	
	2014 A-SSCC [18]		2013 JSSC [10]		2013 JSSC [11]		2013 A-SSCC [6]	2012 TCAS-I [7]	2014 A-SSCC [8]	2013 ISSCC [9]
RF Freq. (GHz)	0.76-0.96	2.4-2.5	0.36-0.51	2.36-2.5	2.4 (TRX)	0.9 (TX)	2.4	2.4	0.169/0.3/0.4/0.9	0.3/0.4/0.8-0.9
BW (MHz)	1/2/10		0.15-3		0.05/1		-	2	0.2	0.9
Modulation type	OFDM (DQPSK)		DQPSK/MSK		DQPSK/ GFSK	FSK	GMSK	-	FSK/ GFSK	FSK/ 3ASK
S_{11} (dB)	-28	-18	-16	-22	-	-	-	-	-	-
RX NF (dB)	5.1	4.2	3.9	4.4	6	-	5.3-5.8	6.2	6	4.5/5.5
RX In-band IIP3 (dBm)	-17*	-19*	-29.4	-26.6	-	-	-	-11**	-	-23
RX IRR (dBc)	48	48	26		-	-	34	22.4	48	60
3rd TRX HRR (dBc)	60 (RX)	-	-	-	-	-	-	-	49.6/51 (TX)	-
TX OP1dB (dBm)	16.3	14.8	2.1	/0.8	5	-3	11	5	13	18
PAPR (dB)	6/9	6	-	-	-	-	-	-	-	-
EVM	3.7%	3.9%	-	8%	10%	-	5.7%	5	-	8
PN (dBc/Hz)	-121.1	-121.7	-121.5		-107	-100	-126†	-107	-128	-125
$P_{DC, RX}$ (mW)	19.1	22.1	15.8	16.6	6.5	-	44.4	25.2	9.84	45
$P_{DC, TX}$ @OP1dB (mW)	183	127.8	13.2	18	14.5	2.5	127.3	23.58 @0dBm	99	252
$P_{DC, PLL}$ (mW)	11.1	20.5	-	-	-	-	-	9.72	2.16	-
Technology (nm)	180		180		130		55	180	65	140
Area (mm^2)	15.7		16		5.9		9.4	3.9	3	5.5

* At 65dB high gain mode. ** Only the LNA with 24dB gain. † At 3MHz offset with 6GHz carrier.

List of figures and tables