Impact of Aging Phenomena on Latches' Robustness

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***Abstract*—In this paper, we analyze the effects of aging mechanisms on the soft error susceptibility of both standard and robust latches. Particularly, we consider Bias Temperature Instability (BTI) affecting both *nMOS* (positive BTI) and *pMOS* (negative BTI), which is considered the most critical aging mechanism threatening the reliability of ICs. Our analyses show that, as an IC ages, BTI increases significantly the susceptibility of both standard latches and low-cost robust latches, whose robustness is based on the increase in the critical charge of their most susceptible node(s). Instead, we will show that BTI minimally affects the soft error susceptibility of more costly robust latches that avoid the generation of soft errors by design. Consequently, our analysis highlights the fact that, in applications mandating the use of low-cost robust latches, designers will have to face the problem of their robustness degradation during IC lifetime. Therefore, for these applications, designers will have to develop proper low-cost solutions to guarantee the minimal required level of robustness during the whole IC lifetime.**

***Index Terms*— Static Latch; Robust Latch; Soft Error; Aging;**

I. Introduction

THE continuous scaling of microelectronic technology enables to keep on increasing system complexity and performance. However, this comes together with an increased vulnerability of ICs to radiation-induced faults [1, 2, 3]. Particularly, it has been proven that single event transients (SETs) affecting storage elements (latches and flip-flops) are by far the major cause of soft errors (SEs) affecting sequential circuits [4, 5]. Consequently, extensive research efforts have been recently devoted to the devising of novel hardening approaches for latches and flips-flops. Robust latches can be divided in two categories, depending on how their increased robustness against SETs is achieved [6]. One category, hereinafter referred to as *category 1*, consists of latches made robust by increasing the capacitance of some of their nodes and/or the driving strength of some transistors (e.g., the latches proposed in [7, 8, 9, 10]). These approaches usually require low area overhead, but do not guarantee complete immunity against SEs. In fact, depending on the hitting particle energy, SETs may still be generated and possibly result in output SEs. The second category of robust latches, hereinafter referred to as *category 2*, consists of latches whose robustness relies on proper modifications of their internal structure, which make them robust regardless of the hitting particle energy (e.g., the latches in [4, 6, 11, 12, 13, 14]). Latches in *category 2* use independent feedback loops to control the output (in some cases through a C-element). This way, a SET affecting one of the loops cannot result in a SE. Therefore, only SETs affecting the input node and satisfying the latch setup and hold times can generate a SE. However, this event has been proven to be very unlikely [8]. Therefore, robust latches in *category 2*) are less vulnerable to SEs than latches in *category 1*). A main drawback of *category 2)* latches, which might limit their use in low-cost applications, is their higher area overhead, power consumption and, in some cases, impact on performance compared to robust latches in *category 1)*.

Together with the increased susceptibility to SETs, aggressively scaled electronics is becoming increasingly prone to aging mechanisms, such as bias temperature instability (BTI), which is considered the primary parametric failure mechanism in modern ICs [15, 16, 17]. Negative BTI (NBTI) and Positive BTI (PBTI) are observed in *pMOS* and *nMOS* transistors, respectively. They cause performance degradation of MOS transistors, when they are ON. For instance, it has been proven that, due to NBTI, the absolute threshold voltage of *pMOS* transistors can increase by more than 50mV over ten years, thus resulting in more than 20% circuit performance degradation [18]. In data-paths of high performance systems, such a performance degradation may exceed circuit time margin, eventually leading to a delay-fault. As a consequence, in the last few years, together with SET modeling, significant efforts have been also devoted to modeling circuit performance degradation over time due to BTI (e.g., [19, 17]). Several approaches have been also proposed to limit the effects of BTI [20, 18], all based on the idea to integrate on-die aging sensors able to detect performance degradation induced by BTI, to then allow the adjustment of the system clock period, thus avoiding that incorrect data are sampled.

In addition, recent works [21, 22, 23, 24, 25] have shown that BTI has a negative impact on the SE susceptibility of ICs. This occurs because BTI significantly reduces the value of the critical charge of nodes of both combinational circuits and SRAMs over time. In fact, as shown in [26], the critical charge

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of a node strongly depends on the value of the restoring current of its pull-up/pull-down networks. Since BTI increases significantly the absolute value of the transistor threshold voltage, it also reduces the value of the restoring current of the affected node. As a result, its critical charge reduces, and the likelihood of SET generation increases noticeably.

As previously mentioned, SETs affecting latches and flip-flops are by far the major cause of SEs affecting sequential circuits. However, to the best of our knowledge, the impact of aging phenomena (namely, BTI) on their SE susceptibility has not been assessed in details so far. In [27], we have presented a preliminary analysis of the effects of NBTI on the soft error rate (SER) of a standard and two robust latches (one robust latch in *category 1* and one robust latch in *category 2*). In this paper, we extend the analysis in [27] to account for the effects of both NBTI and PBTI (BTI) on the SER of the standard and robust latches considered in [27]. We also assess the effect of different stress conditions on the transistors composing the latches. Moreover, we analyze the effects of BTI on the SER of four additional robust latches (two in *category 1* and two in *category 2*) recently proposed in literature.

We show that, during the circuit operating time, BTI may significantly increase the SER of standard latches and that of low-cost robust latches in *category 1*, while it minimally affects the SER of more expensive robust latches in *category 2*. This because robust latches in *category 2* filter out SETs on all their internal and output nodes by design. They are only susceptible to SEs due to SETs occurring at their input node during the latch setup and hold times, which is an unlikely event [8]. It should be noted that hold time is generally negligible for recent latches, and it will not considered in our analysis. Our analysis highlights that, in applications requiring the use of low-cost robust latches in *category 1*, rather than the more robust, but also more costly latches in *category 2*, designers will need to face the problem of the degradation of their robustness over time.

The rest of the paper is organized as follows. In Section II, we give some preliminaries on BTI and soft error rate of latches. In Section III, we analyze the impact of BTI on the critical charge and setup time of a standard and some robust latches in *category 1* and *2*. In Section IV, we analyze the impact of BTI on the SER of the considered latches. Finally, in Section V, we draw some conclusive remarks.

II. Preliminaries on BTI and SER

As discussed in [8], the soft error rate (SER) of a latch can be expressed by the sum of several contributions, each referred to a node of the latch. In turn, SET susceptibility of each node can be expressed as a function of: i) the window-of-vulnerability (*WOV*), which is the time interval within a clock period (T_{CK}) during which a SET hitting the node can propagate till the output of the latch and give rise to a SE; ii) the critical charge (Q_{crit}) of the considered node, that is the amount of charge collected by the hit node that produces a voltage glitch whose amplitude exceeds the logic threshold of the fan-out gate. The total SER for a latch is given by:

$$SER = \sum_{i=1}^{n} \frac{WOV_i}{T_{CK}} \Phi_P k_i \, e^{-\beta \cdot Qcrit(i)}, \quad (1)$$

where $i=1..n$ are the nodes of the latch that may produce an output SE if affected by a SET; κ_i is proportional to the susceptible area of the node i (A_i); Φ_P is the flux of hitting particles ($\Phi_P \cong 56.5/s \cdot m^2$ at sea level [28]); β is a parameter depending on the technology and operating environment [8].

As discussed in [8], SEs caused by SETs affecting the internal/output nodes of a latch are the major contributors to the overall latch SER, while SEs caused by SETs affecting the latch input node have a marginal impact. This is mainly because the *WOV* of the latch input node, which is equal to the latch setup and hold times, is considerably smaller than the *WOV* of the latch internal/output nodes, which is generally equal to latching phase duration $T_{CK}/2$ [8].

Bias Temperature Instability (BTI) causes significant threshold voltage degradation in MOSFET using either Hafnium-dioxide high-k dielectric material or pure Silicon Dioxide (SiO_2) [17]. Negative BTI (NBTI) and Positive BTI (PBTI) are observed in *pMOS* and *nMOS* transistors, respectively. They cause a threshold voltage shift (ΔV_{th}) in MOS transistors when they are ON (stress phase), at elevated temperatures [17]. The BTI-induced degradation is partially recovered when the MOS transistors are OFF (recovery phase). The reaction-diffusion model in [17] allows designers to estimate the threshold voltage increase as a function of technology parameters, operating conditions and time. However, it is not suitable to model long-term BTI degradation. In [29, 25], an analytical model has been proposed that allows designers to estimate the long-term, worst-case threshold voltage shift ΔV_{th} as a function of applied voltage, stress/recovery time and temperature. It is:

$$\Delta V_{th} = \chi \cdot K_{lt} \cdot \sqrt{C_{ox}(V_{dd} - V_{th})} e^{-\frac{E_a}{kT}} (\alpha \Delta t)^n, \quad (2)$$

where C_{ox} is the oxide capacitance, Δt is the operating time, α is the fraction of time in which the considered transistor is under a stress condition, E_a is the interface traps activation energy ($E_a \cong 0.8eV$ [30]), k is the Boltzmann constant, T is the operating temperature, n is a fitting parameter equal to 1/6. The coefficient χ enables to distinguish between PBTI (χ=0.5) and NBTI (χ=1) effects [25, 19, 24], showing that PBTI is less a severe problem than NBTI. By means of the parameter α ($0 \leq \alpha \leq 1$) we are able to account for the effective amount of time during which a device is under stress. It is α=0, if the MOS transistor is always OFF (recovery phase), whereas α=1, if it is always ON (stress phase). Finally, the parameter K_{lt} lumps technology specific and environmental parameters, and has been estimated to be $K_{lt} = 2.7V^{1/2}F^{-1/2}s^{-1/6}$, by fitting the model in [29] with the experimental results reported in [31] for a 32nm High-K CMOS technology.

As introduced before, in this paper we investigate the impact of BTI on the latches' SER that, as shown in (1), depends on the Q_{crit} and on the *WOV* of each latch node.

III. Impact of BTI on Latch Node Critical Charge and Setup Time

We assess the impact of BTI-induced MOS transistor threshold voltage shift (ΔV_{th}) on the Q_{crit} of latch nodes and on the latch setup time (t_{SU}). Particularly, through HSPICE simulations, we analyze how Q_{crit} and t_{SU} vary as a function of operating time and stress ratio. This latter, in turn, depends on the probability to have a logic 1 at the latches' input. In our analysis, we have not evaluated the latches' hold time (t_{hold}) degradation due to BTI, since we have verified that for the considered latches it is $t_{hold} \approx 0$.

A. Simulation Setup

The considered latches are shown in Fig. 1. They are: 1) the latch in [32] (Fig. 1(a)), as an example of standard latch; 2) the robust latches recently proposed in [7], [8] and [10] (Figs. 1(b), 1(c) and (d), respectively) that belong to *category 1*; 3) the robust latches recently proposed in [6] and [14] (Figs. 1(e) and 1(f), respectively) that belong to *category 2*. We have implemented all latches with a 32nm High-K CMOS technology [33], with 1V power supply, 1Ghz clock frequency, and minimum transistor sizes guaranteeing a correct behavior.

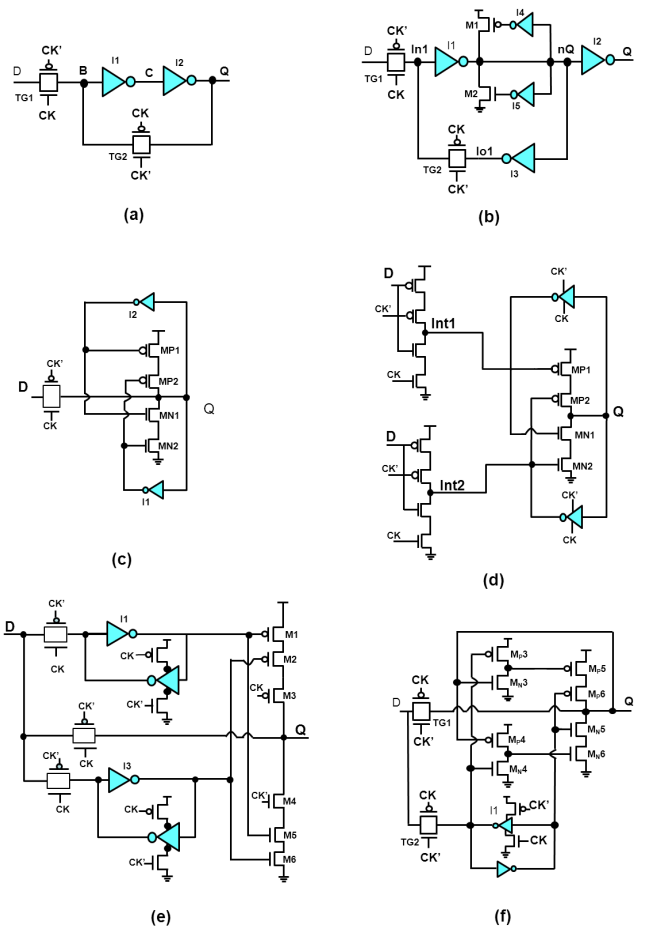

Fig. 1. Schematic representation of the latches considered in our analyses: a) standard latch; b) robust latch of *category 1* in [7]; c) robust latch of *category 1* in [8]; d) robust latch of *category 1* in [10]; e) robust latch of *category 2* in [14]; c) robust latch of *category 2* in [6].

For each latch, we have evaluated only the Q_{crit} of those nodes that, when affected by a SET, may generate a SE. Since these nodes present a finite value of Q_{crit}, they are the only nodes contributing to the SER of a latch. In particular, we have evaluated the Q_{crit} of the following nodes: *B*, *C*, *Q* and *D*, for the standard latch (Fig. 1(a)); *in1*, *nQ*, *Io1* and *D*, for the robust latch in [7] (Fig. 1(b)); *Q* and *D*, for the robust latches in [8] and [10] (Figs. 1(c) and 1(d)). As for the robust latches in *category 2* in [6, 14] (Figs. 1(e) and 1(f)), we have evaluated the Q_{crit} of node *D* only, since SETs affecting all other nodes are completely filtered out.

We have computed the threshold voltage shift ΔV_{th} induced by BTI degradation by utilizing the model in (2), for some representative circuit operating times (Δt=0, 1, 3, 6 years). We have considered an operating time up to 6 years only, because we have verified that the BTI degradation exhibited after 6 years is comparable to that after 10 years of operation, being the maximum difference lower than 2%. In order to account for the impact of different stress ratio on the BTI-induced Q_{crit} variation, we have considered three different probabilities of having a logic 1 at the latches' input ($P_{IN=1}$). Namely, we have evaluated the BTI degradation for $P_{IN=1}$=0.25, $P_{IN=1}$=0.5, and $P_{IN=1}$=0.75.

B. Impact of BTI on the Critical Charge

In Table 1, we report the Q_{crit} values of the nodes of the considered latches, for circuit operating times and input probabilities previously considered. The table also reports the relative reduction of Q_{crit} of each node for the considered circuit operating times, calculated as:

$$\Delta Q_{crit} = 100\ (Q_{crit\_\Delta t=1,3,6} - Q_{crit\_\Delta t=0}) / Q_{crit\_\Delta t=0}.$$

First, for all latches and for all input probabilities, the Q_{crit} of all nodes decreases rapidly during the early stage of lifetime. Particularly, it can be observed that, after only 1 year of operation, the Q_{crit} degradation exceeds 60% of the total degradation experienced after 6 years. After 3 years of operation, it exceeds 90% of the value after 6 years for all nodes and input probabilities. Moreover, considering the standard latch and the robust latches in *category 1*, we can see that node *B* in the standard latch, node *In1* in the latch in [7], and node *Q* in the latches in [8, 10] exhibit the lowest value of Q_{crit} for all considered operating time. This holds true for all considered input probabilities.

It is worth noticing that the relationship among the Q_{crit} of the nodes in the standard latch and in the robust latch in [7] is in accordance with the results reported in [26]. They proved that the critical charge of a circuit node depends much more on the conductance of the gate driving the node (driving strength) than on the node capacitance. In fact, for the standard latch and for the robust latch in [7], the Q_{crit} of the input and output nodes is considerably higher than that of the other internal nodes (i.e., *B* and *C* in the standard latch, *In1* and *Io1* in the latch in [7]). Indeed, these latter are driven by transfer gates, which exhibit a much lower strength than the gates driving the input and output nodes. Moreover, we can

also note that the Q_{crit} of input node *D* is slightly higher than that of the output node *Q*. This because, although both nodes are driven by gates with the same conductance, the node capacitance associated with the input node *D* is slightly higher than that associated to the output node *Q*, which we have assumed loaded by a minimum-sized inverter.

From Table 1, we can observe that all nodes exhibit the highest Q_{crit} degradation for $P_{IN=1}$=0.75, and that the relative difference between different $P_{IN=1}$ is small (always lower than 4%). Moreover, the nodes with the highest reduction in the Q_{crit} value after Δt=6 years are: node *B* in the standard latch (ΔQ_{crit} = -17.4%), node *D* in the robust latch of *category 1* in [7] (ΔQ_{crit} = -20.2%), and node *D* in the robust latches of *category 1* in [8] and [10] (ΔQ_{crit} = -20.3% and 14.8%, respectively). As for the robust latches of *category 2* in [14, 6], their input node, which is their only susceptible node, presents a 16.8% and 20.2% Q_{crit} reduction, respectively.

C. Impact of BTI on Setup Time

We now report some of the simulation results showing how the setup time (t_{SU}) of the considered latches (Fig. 1) increases as a function of circuit operating time Δt. As clarified in Section II, the SER of latches depends linearly on the *WOV* of their nodes. Since the *WOV* of the input node equals the t_{SU} of the latches, we should account for the t_{SU} variation due to BTI to accurately characterize how operating time affects the SER of the latches. Consider that robust latches of *category 2* in [14, 6] can experience SEs only because of SETs affecting their input node during t_{SU}. Thus, for these latches, the t_{SU} variation over time will directly influence their SER. On the other hand, in the standard latch and in the considered robust latches of *category 1* ([7, 8, 10]), the *WOV* of the input node (t_{SU}) is considerably smaller than the *WOV*s of all other nodes (generally equal to $T_{CK}/2$). Therefore, the t_{SU} variation over time will minimally affect the SER of these latches. However, in order to avoid timing violations in aged circuits, such a t_{SU} variation should be taken into account by the designers, especially if the latches are connected to the outputs of critical data-paths.

Fig. 2 shows the values of the t_{SU} of all considered latches, as a function of circuit lifetime Δt, for $P_{IN=1}$=0.5. We can observe that, for all latches, the value of t_{SU} is a monotonic function increasing with the circuit operating time Δt. Particularly, t_{SU} increases with a much higher rate during the first 2-3 years of circuit operation, than during the remaining circuit operating time. In fact, the variation exhibited at Δt = 3 years ranges from 78% to 96% of the total variation after 6 years of operation.

TABLE 1. VALUES OF Q_{CRIT} OF THE NODES OF THE LATCHES IN FIG. 1 AND THEIR RELATIVE REDUCTION AFTER SOME REPRESENTATIVE CIRCUIT OPERATING TIMES AND THREE DIFFERENT PROBABILITIES OF HAVING A LOGIC 1 AT THE LATCHES' INPUT ($P_{IN=1}$=0.25, $P_{IN=1}$=0.5, AND $P_{IN=1}$=0.75).

		Latch Standard				Category 1 Latches								Category 2 Latches	
						Latch in [7]				Latch in [8]		Latch in [10]		Latch in [14]	Latch in [6]
		D	B	C	Q	D	In1	nQ	Io1	D	Q	D	Q	D	D
Δt=0	Q_{crit} (fC)	13.68	5.12	8.55	10.53	13.68	6.58	16.67	12.61	13.68	10.57	14.02	10.58	14.93	14.01
Δt=1 year	Q_{crit} (fC)	12.08	4.54	7.93	9.83	12.08	5.75	15.81	11.76	11.97	9.53	12.08	9.52	13.45	11.97
$P_{IN=1}$=0.5	ΔQ_{crit} (%)	-11.7	-11.3	-7.3	-6.7	-11.7	-12.7	-5.1	-6.7	-12.5	-9.8	-13.8	-10.0	-11.0	-14.5
Δt=3 years	Q_{crit} (fC)	11.29	4.35	7.86	9.80	11.29	5.59	15.65	11.62	11.34	9.29	11.51	9.29	12.77	11.50
$P_{IN=1}$=0.5	ΔQ_{crit} (%)	-17.5	-15.0	-8.1	-6.9	-17.5	-15.0	-6.0	-7.9	-17.1	-12.1	-17.9	-12.1	-14.5	-17.8
Δt=6 years	Q_{crit} (fC)	11.17	4.29	7.81	9.77	11.17	5.48	15.54	11.49	11.23	9.14	11.29	9.12	12.65	11.34
$P_{IN=1}$=0.5	ΔQ_{crit} (%)	-18.3	-16.2	-8.7	-7.3	-18.3	-16.7	-6.7	-8.9	-17.9	-13.5	-19.5	-13.8	-15.3	-19.0
Δt=1 year	Q_{crit} (fC)	12.20	4.60	7.97	9.97	12.20	5.92	15.91	11.91	12.14	9.66	12.29	9.64	13.62	12.31
$P_{IN=1}$=0.25	ΔQ_{crit} (%)	-10.8	-10.1	-6.8	-5.3	-10.8	-10.1	-4.5	-5.5	-11.3	-8.6	-12.4	-8.8	-9.6	-12.1
Δt=3 years	Q_{crit} (fC)	11.51	4.45	7.91	9.89	11.51	5.69	15.77	11.74	11.63	9.43	11.69	9.43	13.01	11.74
$P_{IN=1}$=0.25	ΔQ_{crit} (%)	-15.8	-13.1	-7.5	-6.1	-15.8	-13.5	-5.3	-6.9	-15.0	-10.8	-16.7	-10.9	-13	-16.1
Δt=6 years	Q_{crit} (fC)	11.40	4.39	7.86	9.83	11.40	5.59	15.66	11.63	11.51	9.30	11.57	9.29	12.77	11.57
$P_{IN=1}$=0.25	ΔQ_{crit} (%)	-16.7	-14.3	-8.1	-6.7	-16.7	-15.0	-6.9	-7.8	-15.8	-12.0	-17.5	-12.1	-14.5	-17.3
Δt=1 year	Q_{crit} (fC)	11.74	4.47	7.91	9.82	11.74	5.69	15.77	11.63	11.69	9.45	11.97	9.44	12.99	11.80
$P_{IN=1}$=0.75	ΔQ_{crit} (%)	-14.2	-12.7	-7.5	-6.8	-14.2	-13.4	-5.3	-7.8	-14.6	-10.6	-14.6	-10.7	-14.9	-15.7
Δt=3 years	Q_{crit} (fC)	11.17	4.30	7.83	9.80	11.17	5.52	15.59	11.55	11.21	9.21	11.4	9.2	12.54	11.40
$P_{IN=1}$=0.75	ΔQ_{crit} (%)	-18.3	-16.0	-8.4	-7.0	-18.3	-16.1	-6.4	-8.4	-18.1	-12.8	-18.7	-13.1	-16.0	-18.6
Δt=6 years	Q_{crit} (fC)	10.94	4.23	7.77	9.75	10.94	5.41	15.46	11.41	11.06	9.04	11.17	9.01	12.43	11.17
$P_{IN=1}$=0.75	ΔQ_{crit} (%)	-20	17.4	-9.1	-9.1	-20.0	-17.7	-7.2	-9.5	-19.2	-14.5	-20.3	-14.8	-16.8	-20.2

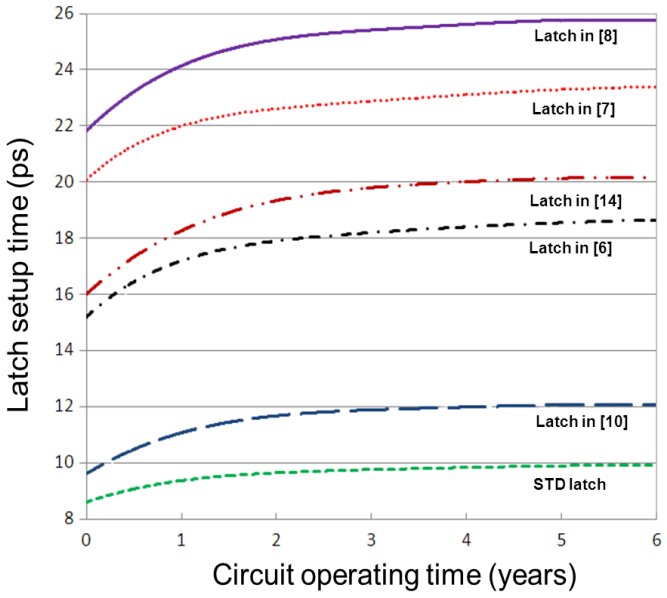

Fig. 2. Values of the setup time of the considered latches as a function of circuit operating time, for the case of having a logic 1 at the latches' input with a 50% probability (i.e., $P_{IN=1}$=0.5).

TABLE 2. VALUES OF T_{SU} OF THE LATCHES IN FIG. 1 AND THEIR RELATIVE INCREASE AFTER SOME REPRESENTATIVE CIRCUIT OPERATING TIMES, AND FOR THREE DIFFERENT INPUT PROBABILITIES ($P_{IN=1}$).

		Latch STD	Latch in [7]	Latch in [8]	Latch in [10]	Latch in [14]	Latch in [6]
Δt=0	t_{SU} (ps)	8.60	22.8	31.2	13.0	18.7	17.3
Δt=1 yr $P_{IN=1}$=0.5	t_{SU} (ps)	9.37	25.1	35.1	14.6	20.5	18.8
	Δt_{SU} (%)	9.0	10.3	12.5	12.3	9.6	8.7
Δt=3 yrs $P_{IN=1}$=0.5	t_{SU} (ps)	9.77	26.2	36.3	15.8	21.2	19.6
	Δt_{SU} (%)	13.6	15.2	16.3	21.5	13.4	13.3
Δt=6 yrs $P_{IN=1}$=0.5	t_{SU} (ps)	9.93	26.7	36.5	16.6	21.7	20.2
	Δt_{SU} (%)	15.5	17.4	17.0	27.7	16.0	16.8
Δt=1 yr $P_{IN=1}$ = 0.25	t_{SU} (ps)	9.1	25.9	36.6	14.2	19.9	19.2
	Δt_{SU} (%)	5.8	14.1	17.3	9.2	7.2	11.0
Δt=3 yrs $P_{IN=1}$ = 0.25	t_{SU} (ps)	9.4	27.3	39.2	15.0	20.9	20.3
	Δt_{SU} (%)	9.3	20.0	25.6	15.6	12.4	17.6
Δt=6 yrs $P_{IN=1}$ = 0.25	t_{SU} (ps)	9.7	27.6	40.3	15.3	21.4	21.1
	Δt_{SU} (%)	12.8	21.5	29.2	17.7	15.1	22.1
Δt=1 yr $P_{IN=1}$ = 0.75	t_{SU} (ps)	9.5	24.6	32.3	15.3	20.2	18.5
	Δt_{SU} (%)	10.7	8.3	3.7	17.7	8.6	6.8
Δt=3 yrs $P_{IN=1}$ = 0.75	t_{SU} (ps)	10.2	25.7	32.75	17.1	21.5	19.2
	Δt_{SU} (%)	18.6	12.8	5	31.5	15.6	10.8
Δt=6 yrs $P_{IN=1}$ = 0.75	t_{SU} (ps)	10.3	26.0	32.8	18.2	22.1	19.3
	Δt_{SU} (%)	19.8	14.3	5.3	40.0	18.8	11.4

More in details, Table 2 reports the t_{SU} values of the considered latches for some representative circuit operating times (Δt=0, 1, 3, 6 years), and three different probabilities of having a logic 1 at the latches' input ($P_{IN=1}$=0.25, $P_{IN=1}$=0.5, and $P_{IN=1}$=0.75). The table also reports the relative increase of the t_{SU} of each latch for the considered circuit operating times, calculated as:

$$\Delta t_{SU} = 100\ (t_{SU\_\Delta t=1,3,6} - t_{SU\_\Delta t=0}) / t_{SU\_\Delta t=0}.$$

We can observe that latches in [7], [8] and [6] experience their maximum t_{SU} increase for $P_{IN=1}$=0.25, whereas for all other latches, the maximum t_{SU} increase is exhibited for $P_{IN=1}$=0.75. After Δt=6 years of circuit operating time, the compared latches present a t_{SU} increase ranging from 18.8% (latch in [14]) to 40% (latch in [10]). Designers should consider such a t_{SU} variation in order to avoid timing violations during circuit lifetime, especially if the latches are connected to the output of critical data-paths.

IV. IMPACT OF BTI ON LATCH SER

We evaluate the SER of the considered latches as a function of the circuit operating time (Δt), for the considered $P_{IN=1}$ probabilities. As shown in (1), for a given latch, the total SER is the sum of the SER of each node that, if affected by a SET, may produce a SE. Therefore, the SER of the analyzed latches will be expressed by the sum of: the SER of nodes *B*, *C*, *Q* and *D*, for the standard latch (Fig. 1(a)); the SER of nodes *in1*, *nQ*, *Io1* and *D*, for the robust latch in [7] (Fig. 1(b)); the SER of nodes *Q* and *D*, for the robust latches in [8, 10] (Figs. 1(c) and 1(d)); the SER of node *D* only (since SETs on other nodes of these latches are filtered out), for the robust latches in [14, 6] (Fig. 1(e) and 1(f)).

In Table 3, we report the nodes *i* contributing to the SER of the considered latches, together with the expressions of the WOV_i and parameter k_i, (reported in the 3rd and 4th columns, respectively). As clarified before, parameter k_i is proportional to the susceptible area of node *i* (A_i). As for the flux of hitting particles Φ_P in (1), we considered $\Phi_P \cong 56.5/s{\cdot}m^2$ [28]. Finally, for the considered 32nm CMOS technology, we have derived the value of parameter β from [34]. In particular, for our analysis we have considered $\beta = 90{\times}10^{12}$ *1/C*.

More in details, according to the expressions of the WOVs and parameter *k* reported in Table 3, we can express the SER of the standard latch (SER_{STD}) and of the robust latches in [7, 8, 10, 14, 6] ($SER_{[7, 8, 10, 14, 6]}$) as follows:

$$SER_{STD} = \Phi_P\left(\frac{t_{setup(std)}}{T_{CK}} A_D e^{-\beta \cdot Q_{crit(D)}} + \frac{1}{2} A_B e^{-\beta \cdot Q_{crit(B)}} + \frac{1}{2} A_C e^{-\beta \cdot Q_{crit(C)}} + \frac{1}{2} A_Q e^{-\beta \cdot Q_{crit(Q)}}\right) \quad (3)$$

$$SER_{[7]} = \Phi_P\left(\frac{t_{setup[7]}}{T_{CK}} A_D e^{-\beta \cdot Q_{crit(D)}} + \frac{1}{2} A_{In1} e^{-\beta \cdot Q_{crit(In1)}} + \frac{1}{2} A_{nq} e^{-\beta \cdot Q_{crit(nq)}} + \frac{1}{2} A_{Io1} e^{-\beta \cdot Q_{crit(Io1)}}\right) \quad (4)$$

$$SER_{[8]} = \Phi_P\left(\frac{t_{setup[8]}}{T_{CK}} A_D e^{-\beta \cdot Q_{crit}(D)} + \frac{1}{2} A_Q e^{-\beta \cdot Q_{crit}(Q)}\right) \quad (5)$$

$$SER_{[10]} = \Phi_P\left(\frac{t_{setup[10]}}{T_{CK}} A_D e^{-\beta \cdot Q_{crit}(D)} + \frac{1}{2} A_Q e^{-\beta \cdot Q_{crit}(Q)}\right) \quad (6)$$

$$SER_{[14]} = \Phi_P \frac{t_{setup[14]}}{T_{CK}} A_D e^{-\beta \cdot Q_{crit}(D)} \quad (7)$$

$$SER_{[6]} = \Phi_P \frac{t_{setup[6]}}{T_{CK}} A_D e^{-\beta \cdot Q_{crit}(D)} \quad (8)$$

TABLE 3. EXPRESSIONS OF WOV AND PARAMETER K FOR THE NODES OF THE LATCHES IN FIG. 1.

Latch	Node i	WOV_i	k_i
Standard	D	$t_{SU\ (std)}$	A_D=9.22×10^{-15} m^2
	B	T_{CK}/2	A_B=9.22×10^{-15} m^2
	C	T_{CK}/2	A_C=3.07×10^{-15} m^2
	Q	T_{CK}/2	A_Q =3.07×10^{-15} m^2
in [7]	D	$t_{SU\ [7]}$	A_D =9.2×10^{-15} m^2
	In1	T_{CK}/2	A_{In1}=9.21×10^{-15} m^2
	nq	T_{CK}/2	A_{nq}=3.07×10^{-15} m^2
	Io1	T_{CK}/2	A_{Io1}=3.07×10^{-15} m^2
in [8]	D	$t_{SU\ [8]}$	A_D=1.23×10^{-14} m^2
	Q	T_{CK}/2	A_Q=1.43×10^{-14} m^2
in [10]	D	$t_{SU\ [10]}$	A_D=1.94×10^{-14} m^2
	Q	T_{CK}/2	A_Q=1.23×10^{-14} m^2
in [14]	D	$t_{SU\ [14]}$	A_D=1.54×10^{-14} m^2
in [6]	D	$t_{SU\ [6]}$	A_D=1.23×10^{-14} m^2

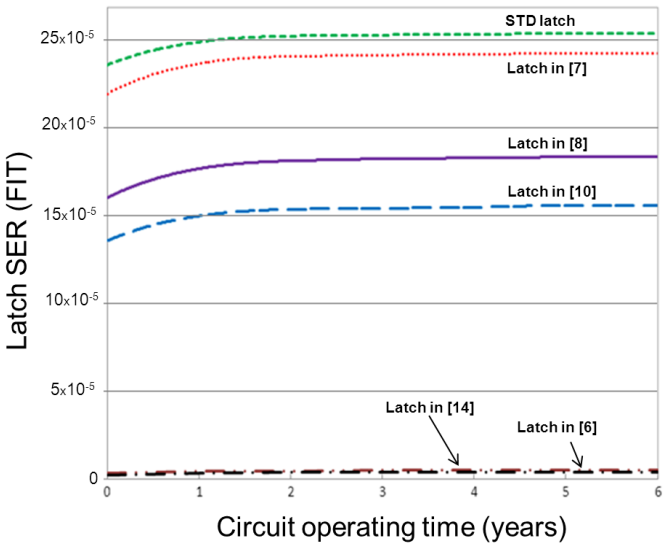

Fig. 3. Values of the SER of the considered latches as a function of circuit operating time, for the case of having a logic 1 at the latches' input with a 50% probability (i.e., $P_{IN=1}$=0.5).

In Fig. 3, we report the obtained trend of the SER for all the considered latches as a function of Δt, for $P_{IN=1}$=0.5. We can see that, as expected, the SER increases with Δt for all latches. During the first 2 years of circuit operation, SER degradation rate is much higher than during the remaining operating time. For all latches, after only 2 years, the SER degradation exceeds 90% of the total degradation exhibited after 6 years of operation. We can also observe that, during the whole circuit lifetime, the SER of the robust latches in [6, 14] (in *category 2*) is approximately one order of magnitude lower than the SER of the standard latch and the robust latches in [7, 8, 10] (in *category 1*). Nonetheless, the SER of the robust latches in [7, 8, 10] are all lower than that of the standard latch along the whole circuit lifetime.

These results show that, as expected, the latches in [6, 14] are much more robust than the standard latch and the robust latches in [7, 8, 10]. Moreover, over the circuit operating time, the SER increase experienced by the latches in [6, 14] is negligible compared to that of the standard latch and the robust latches in [7, 8, 10].

Table 4 reports the SER values of the considered latches for Δt = 0, 1, 3, 6 years, and the considered probabilities to have a logic 1 at the latches' input ($P_{IN=1}$=0.25, $P_{IN=1}$=0.5, and $P_{IN=1}$=0.75). For each circuit operating time, the table also reports the ratio between the SER increase of the standard latch and the latches in [7, 8, 10] over the SER increase of the latch in [6] (denoted by $R_{\Delta SER\_[6]}$), and over the SER increase of the latch in [14] (denoted by $R_{\Delta SER\_[14]}$). In particular, we calculated:

$$R_{\Delta SER\ [6,14]} = \frac{\Delta SER_{STD;[7,8,10]}}{\Delta SER_{[6,14]}}; \text{ with } \Delta SER = \frac{SER_{\Delta t=1,3,6\ years} - SER_{\Delta t=0}}{SER_{\Delta t=0}}.$$

The results reported in Table 4 show that, after 6 years of circuit operation, the SER increase of the considered robust latches in *category 2* (i.e., those in [6, 14]) is at least 10 times smaller than the SER increase of the standard latch, and of the other considered robust latches in *category 1* (i.e., those in [7, 8, 10]).

Therefore, as highlighted before, the impact of BTI on the SER of robust latches in *category 2* is negligible compared to the impact of BTI on the SER of standard and low-cost robust latches in *category 1*. Finally, we can see that the effect of different $P_{IN=1}$ is limited, being the relative SER difference between the case with $P_{IN=1}$=0.75 (highest SER) and $P_{IN=1}$=0.25 (lowest SER) less than 1.5%.

V. CONCLUSIONS

We have analyzed the effects of bias temperature instability (BTI) on the soft error rate of both standard and robust latches. We have shown that the SER of both standard latches and low-cost robust latches, whose robustness relies on the increase of the critical charge of their most susceptible node(s), degrades considerably over time due to BTI. Instead, as for the SER of the most costly robust latches, which avoid

the generation of soft errors by design, we have proven that it is minimally affected by BTI. For all considered latches, after only 2 years, the SER degradation exceeds 90% of the total degradation exhibited after 6 years of operation. We have also shown that the effect of different input statistics on latch SER is less than 1.5%. The obtained results highlight the fact that, in applications mandating the use of low-cost robust latches, designers will have to develop proper innovative low-cost solutions to counteract SER degradation over time, thus guaranteeing the minimal required level of robustness during the whole IC lifetime.

TABLE 4. SER OF THE LATCHES IN FIG. 1, AND RATIO BETWEEN THE SER INCREASE OF THE STANDARD AND THE LATCHES IN [7, 8, 10] OVER THE SER INCREASE OF THE LATCHES IN [6, 14], AND FOR THREE DIFFERENT PROBABILITIES OF HAVING A LOGIC 1 AT THE LATCHES' INPUT ($P_{IN=1}$).

		Latch STD	Latch in [7]	Latch in [8]	Latch in [10]	Latch in [14]	Latch in [6]
Δt=0	SER (FIT)	2.37×10^{-4}	2.21×10^{-4}	1.61×10^{-4}	1.37×10^{-4}	4.19×10^{-6}	3.38×10^{-6}
Δt=1 yr $P_{IN=1}$=0.5	SER (FIT)	2.51×10^{-4}	2.39×10^{-4}	1.78×10^{-4}	1.51×10^{-4}	5.25×10^{-6}	4.40×10^{-6}
	$R_{ASER\_[6]}$	13.2	17.4	16.7	14.2	NA	NA
	$R_{ASER\_[14]}$	12.8	16.9	16.2	13.8	NA	NA
Δt=3 yrs $P_{IN=1}$=0.5	SER (FIT)	2.54×10^{-4}	2.42×10^{-4}	1.83×10^{-4}	1.55×10^{-4}	5.78×10^{-6}	4.79×10^{-6}
	$R_{ASER-[6]}$	12.0	15.4	15.3	13.0	NA	NA
	$R_{ASER\_[14]}$	10.7	13.7	13.7	11.6	NA	NA
Δt=6 yrs $P_{IN=1}$=0.5	SER (FIT)	2.55×10^{-4}	2.45×10^{-4}	1.85×10^{-4}	1.58×10^{-4}	5.97×10^{-6}	5.01×10^{-6}
	$R_{ASER\_[6]}$	11.2	14.9	14.8	12.9	NA	NA
	$R_{ASER\_[14]}$	10.3	13.7	13.5	11.9	NA	NA
Δt=1 yr $P_{IN=1}$=0.25	SER (FIT)	2.49×10^{-4}	2.35×10^{-4}	1.77×10^{-4}	1.49×10^{-4}	5.03×10^{-6}	4.36×10^{-6}
	$R_{ASER\_[6]}$	12.1	14.9	15.7	12.9	NA	NA
	$R_{ASER\_[14]}$	13.8	17.1	18.0	14.8	NA	NA
Δt=3 yrs $P_{IN=1}$=0.25	SER (FIT)	2.52×10^{-4}	2.40×10^{-4}	1.81×10^{-4}	1.53×10^{-4}	5.58×10^{-6}	4.87×10^{-6}
	$R_{ASER-[6]}$	10.0	13.1	13.4	10.8	NA	NA
	$R_{ASER\_[14]}$	10.6	13.9	14.2	11.5	NA	NA
Δt=6 yrs $P_{IN=1}$=0.25	SER (FIT)	2.54×10^{-4}	2.43×10^{-4}	1.84×10^{-4}	1.55×10^{-4}	5.83×10^{-6}	5.13×10^{-6}
	$R_{ASER\_[6]}$	9.4	12.5	12.7	10.3	NA	NA
	$R_{ASER\_[14]}$	9.8	13.2	13.4	10.9	NA	NA
Δt=1 yr $P_{IN=1}$=0.75	SER (FIT)	2.52×10^{-4}	2.40×10^{-4}	1.79×10^{-4}	1.53×10^{-4}	5.39×10^{-6}	4.39×10^{-6}
	$R_{ASER\_[6]}$	14.6	19.2	17.6	15.7	NA	NA
	$R_{ASER\_[14]}$	12.1	15.9	14.6	13.1	NA	NA
Δt=3 yrs $P_{IN=1}$=0.75	SER (FIT)	2.55×10^{-4}	2.44×10^{-4}	1.83×10^{-4}	1.57×10^{-4}	5.98×10^{-6}	4.73×10^{-6}
	$R_{ASER-[6]}$	13.4	17.2	16.3	15.0	NA	NA
	$R_{ASER\_[14]}$	10.0	12.8	12.2	11.2	NA	NA
Δt=6 yrs $P_{IN=1}$=0.75	SER (FIT)	2.57×10^{-4}	2.47×10^{-4}	1.86×10^{-4}	1.60×10^{-4}	6.21×10^{-6}	4.85×10^{-6}
	$R_{ASER\_[6]}$	13.2	17.5	16.9	15.8	NA	NA
	$R_{ASER\_[14]}$	9.6	12.7	12.3	11.4	NA	NA

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