Design of Millimeter-Wave Bandpass Filters with Broad Bandwidth in Si-based Technology

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***Abstract*—In this work, a novel design approach is proposed for on-chip bandpass filter (BPF) design with improved passband flatness and stopband suppression. The proposed approach simply uses a combination of meander-line structures with metal-insulator-metal (MIM) capacitors. To demonstrate the insight of this approach, a simplified equivalent *LC*-circuit model is used for theoretical analysis. Using the analyzed results as a guideline along with a full-wave electromagnetic (EM) simulator, two BPFs are designed and implemented in a standard 0.13-μm (Bi)-CMOS technology. The measured results show that good agreements between EM simulated and measured results are achieved. For the 1st BPF, the return loss is better than 10 dB from 13.5 to 32 GHz, which indicates a fractional bandwidth (FBW) of more than 78%. In addition, the minimum insertion loss of 2.3 dB is achieved within the frequency range from 17 GHz to 27 GHz and the in-band magnitude ripple is less than 0.1 dB. The chip size of this design, excluding the pads, is 0.148 mm^2. To demonstrate a miniaturized design, a 2nd design example is given. The return loss is better than 10 dB from 17.3 to 35.9 GHz, which indicates a FBW of more than 70%. In addition, the minimum insertion loss of 2.6 dB is achieved within the frequency range from 21.4 GHz to 27.7 GHz and the in-band magnitude ripple is less than 0.1 dB. The chip size of the 2nd design, excluding the pads, is only 0.066 mm^2.**

***Index Terms*—Bandpass filter, Bi-CMOS, miniaturization, on-chip resonator, RFIC, millimeter-wave, Silicon-Germanium (SiGe), wideband.**

I. Introduction

The trend towards to "Big Data" is rapidly becoming the way of the future and it has the potential to significantly change the way how our daily lives are managed. One major challenge for enabling "Big Data" is how to move enormous amount of data in and out of data center. To tackle this challenge, one of the cost-effective ways is to utilize high-speed wireless links, which requires not only sophisticated modulation scheme, such as 256 QAM, but also very broad radio spectrum. For this reason, the frequency bands at quasi-millimeter-wave (quasi-mm-Wave) and millimeter-wave (mm-Wave) region have been widely used to support the required high-speed data transfer. Among different transceiver architectures, frequency-interleaved (also known as frequency-multiplexed) structure has been presented in the literature, as an alternative to time-interleaving, to support on-chip solutions of next-generation high-speed wireless and photonic applications [1]. Among different building blocks in such a system, bandpass filter (BPF) is perhaps the most indispensable component, which is used to not only pass wanted signals with minimum insertion loss across ultra-wideband, but also reject unwanted interference at stopband. Although the recent advance in on-chip BPF design for quasi-mm-Wave and mm-Wave applications has resulted in several breakthroughs [2]-[16], novel design methodologies are still required to further enhance performance. The conventional design approach based on lumped elements is well suitable for miniaturized design, but it may not be feasible for filter design operating at quasi-mm-Wave and mm-Wave frequencies due to layout-constraint design [2]-[3]. In contrast, the distributed-element-based approach is widely used for filter design operating at this frequency region, but it often results in a relatively large die area [4]-[16]. Even though the physical dimensions of a transmission line are inherently reduced with increased operation frequency, it is still relatively large at quasi-mm-Wave region.

In this work, a novel quasi-lumped-element-based design approach is proposed. Using this design approach, two ultra-broadband on-chip BPFs are designed and implemented in a standard 0.13-μm (Bi)-CMOS technology. Based on the measured results, the 1st designed BPF has achieved a remarkable performance, including a broad fractional bandwidth (FBW) of 78% and minimum insertion loss of 2.3 dB. The chip size for this design, excluding the pads, are only 0.148 mm^2 (0.37 × 0.4 mm^2). To further reduce the physical dimensions of the BPF without significantly deteriorating other performance, the 2nd design is presented using vertically folded metal strips. The measured results have shown that the return loss of the 2nd design is better than 10 dB from 17.3 to 35.9 GHz, which indicates an FBW of more than 70%. In addition, the minimum insertion loss of 2.6 dB is achieved within the frequency range from 21.4 GHz to 27.7 GHz and the in-band magnitude ripple is less than 0.1 dB.

II. Analysis and Synthesis of Broadband BPFs

The generic idea of the presented design approach is shown in Fig. 1. As illustrated, a BPF can be constructed by loading two shunt stubs (also known as notches). The stubs are used to form the low- and high-frequency stopband, while the frequency between these two notches can be used as passband. Carefully selecting the locations of two notches,

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it is feasible to build a BPF with broad passband and sharp cut-off selectivity.

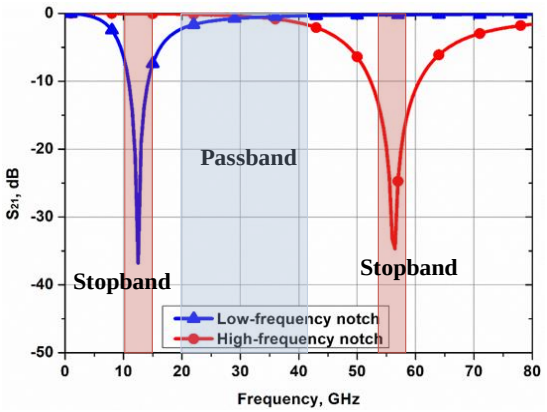

Fig. 1. Indication of the generic idea used for BPF design in this work.

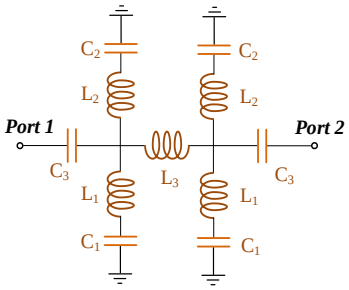

Fig. 2. Simplified lumped-element circuit model used for BPF design.

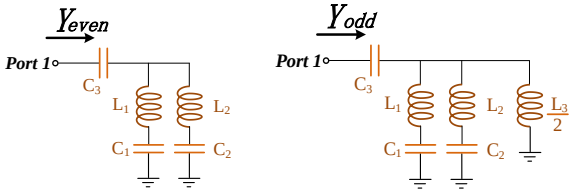

Fig. 3. Simplified equivalent circuit models (a) even-mode excitation, (b) odd-mode excitation.

A. Lumped-Element Equivalent-Circuit Model and Analysis of BPF Designs

To apply the above-mentioned idea for BPF design in practice, a simplified lumped-element model is presented in Fig. 2, which can be used to guide the design. As can be seen, the circuit model consists of the lumped elements, namely L_1, L_2, L_3, and C_1, C_2, C_3, while L_1, L_2 and C_1, C_2 are used to generate the required notch frequencies. The element L_3 is used to model the interconnection between the pair of notch filter, while C_3 is used to form a capacitive feeding of the BPF, so that low-frequency components can be blocked. It is obvious that due to the *LC*-series circuit of L_1, C_1 and L_2, C_2, resonances at certain frequencies will happen under the conditions of:

$$j\omega L + \frac{1}{j\omega C} = 0 \tag{1}$$

Equation (1) indicates that the resonance will stop the signals from traveling, which lead to transmission zeros as indicated in Fig. 1. The positions of two transmission zeros are found to be located at:

$$f_{tz1} = \frac{1}{2\pi\sqrt{L_1C_1}}, \text{ and } f_{tz2} = \frac{1}{2\pi\sqrt{L_2C_2}} \tag{2}$$

It is clearly seen from (2) that the presented circuit model can produce two transmission zeros (TZs). In addition, the equation (2) also indicates that the two TZs can be adjusted independently, which brings another degree of design flexibility in practice.

To design a filter, one needs to know two things: (1) the positions of resonant poles (also refer to resonant modes) and transmission zeros, and (2) the FBW and the in-band ripple level. Since the circuit is fully symmetrical, it is possible to describe its transmission characteristics by adopting the even- and odd-mode analysis method. The even- and odd-mode equivalent circuits are shown in Figs. 3(a) and 3(b), respectively.

For the even-mode, the symmetric plane in the middle is considered as a perfect magnetic wall, while for the odd-mode, the middle plane is treated as a perfect electrical wall (virtual ground). The circuit can be modeled as a reciprocal two-port network by its admittance matrix [*Y*], which can be written as [18]:

$$[Y] = \begin{pmatrix} \frac{Y_{even}+Y_{odd}}{2} & \frac{Y_{even}-Y_{odd}}{2} \\ \frac{Y_{even}-Y_{odd}}{2} & \frac{Y_{even}+Y_{odd}}{2} \end{pmatrix} \tag{3}$$

where Y_{even} and Y_{odd} represent the even- and odd-mode input admittances:

$$Y_{even} = \frac{1}{\frac{1}{j\omega C_3} + \frac{1}{\frac{j\omega C_1}{1-\omega^2 L_1 C_1} + \frac{j\omega C_2}{1-\omega^2 L_2 C_2}}} \tag{4}$$

$$Y_{odd} = \frac{1}{\frac{1}{j\omega C_3} + \frac{1}{\frac{j\omega C_1}{1-\omega^2 L_1 C_1} + \frac{j\omega C_2}{1-\omega^2 L_2 C_2} + \frac{2}{j\omega L_3}}} \tag{5}$$

When Y_{even} = 0, two even-mode resonant modes can be calculated as [19]:

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{C_1+C_2}{C_1C_2L_1+C_1C_2L_2}}, \text{ and } f_1' = 0 \tag{6}$$

Similarly, when Y_{odd} = 0, two odd-mode resonant modes can be found at:

$$f_2 = \frac{1}{2\pi}\sqrt{\frac{n+\sqrt{n^2-4m}}{2m}}, \text{ and } f_2' = \frac{1}{2\pi}\sqrt{\frac{n-\sqrt{n^2-4m}}{2m}} \tag{7}$$

where

$$m = \frac{C_1C_2L_2L_3}{2} + \frac{C_1C_2L_1L_3}{2} + C_1C_2L_1L_2 \tag{8}$$

$$n = \frac{C_1L_3}{2} + \frac{C_2L_3}{2} + C_1L_1 + C_2L_2 \tag{9}$$

The locations of the three resonant modes derived from (6) and (7) are plotted as a function of inductance value of L_3, which is shown in Fig. 4. As can be seen, the resonant pole f_2 is more sensitive to the variation of inductance of L_3 than the others. On the other hand, the resonant pole f_1 is independent to this variation. Thus, by carefully selecting the value for L_3, the bandwidth of the filter can be adjusted accordingly based on different design specifications. It is noted that the other resonant pole f_2' is not used to construct the passband of the BPF in this case, which is placed at the low-frequency stopband. As indicated in Fig. 4 and will be shown in the later sections, this additional resonant pole can be placed very close to the low-frequency TZ, f_{TZ1}. As a result, the unwanted low-frequency spur will be suppressed by f_{TZ1}. This is particularly true, while all inductors are replaced by lossy metal strips in silicon technology.

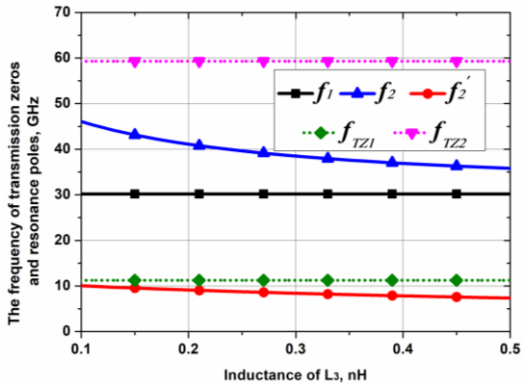

Fig. 4. Resonant poles and TZ frequencies as a function of inductance of L_3. Note: while L_1 = 0.12 nH, L_2 = 0.4 nH, C_1 = 60 fF, C_2 = 0.5 pF, C_3 = 0.4 pF.

B. *Synthesis of BPF Characteristics*

On the other hand, the characteristics of the BPF can be synthesized using the admittance matrix [Y]. It is apparent that the proposed filter is a dual-mode BPF, which is constructed by two modes ω_1 and ω_2. The coupling coefficient k between ω_1 and ω_2 can be expressed by

$$k = \frac{Y_{12}}{b} = \frac{Y_{even} - Y_{odd}}{2b} \tag{10}$$

$$b = \frac{\omega_o}{2} \cdot \frac{\partial \mathrm{Im}(Y_{11})}{\partial \omega}\Big|_{\omega=\omega_o} \tag{11}$$

where k is the coupling coefficient; b is the slope parameter of the filter; ω_0 is the center frequency of the passband, which should be predetermined by:

$$\omega_0 = 2\pi f_o = \pi \cdot (f_{even} + f_{odd}) \tag{12}$$

In this case, the value of b is fixed, and k varies against frequency. For a dual-mode filter, the external quality factor is related to the fractional bandwidth FBW and the in-band ripple level. The external quality factor can be expressed as:

$$Q_{ex} = \frac{b}{(J_{01}^2/Y_o)} = \frac{g_0 g_1}{FBW} \tag{13}$$

$$J_{01} = \sqrt{\frac{Y_o b \cdot FBW}{g_0 g_1}} \tag{14}$$

where g_0, g_1 refer to the basic element value of a conventional 2-stage lowpass filter prototype; J_{01} is the value of the admittance inverter at the input/output port. The fractional bandwidth can be calculated using $FBW = \Delta/f_o$, where Δ is the actual bandwidth of the BPF. When J_{01} is determined, the cascaded capacitor C_3 at the input/output port can be calculated as:

$$C_3 = \frac{J_{01}}{\omega_o \sqrt{1-(J_{01}/Y_o)^2}} \tag{15}$$

It is clearly seen that apart from resonant poles and TZs, the BPF characteristics, such as in-band ripple level, bandwidth, external quality factor and coupling coefficient, are also largely related to the design parameters L_1, L_2, L_3, and C_1, C_2, C_3. When the lowpass filter prototype is chosen, the admittance inverter at the input/output port J_{01} can be calculated using the slope parameter b, and then Q_{ex}, FBW and C_3 can be obtained using (13), (14) and (15). Therefore, it is possible to design BPF with flexible and width bandwidth, sharp passband selectivity and in-band characteristics.

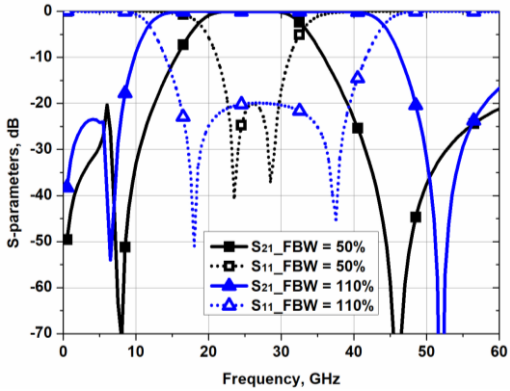

Fig. 5. Two different wideband BPFs with 50% and 110% *FBW*.

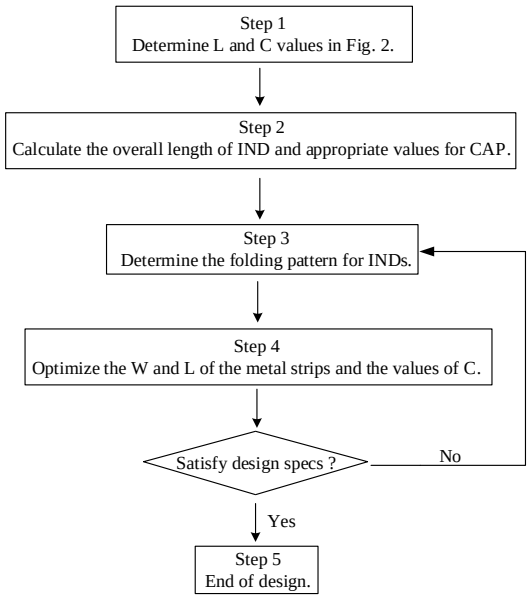

Fig. 6. Design flow used in this work.

Based on the synthesis of BPF characteristics above, wide operating bandwidth can be achieved by selecting a relatively lower Q_{ex} and thus larger value of J_{01}. In this case, the slope parameter of the filter b should be larger as well, which can be obtained from the derivative of Y_{11}. As a design example, two BPFs with different FBWs are designed, whose S-parameters are shown in Fig. 5. The target FBW of two BPFs are 50% and 110%, respectively, and the in-band ripple level is 0.043 dB (return loss = -20 dB). In this case, the basic element values for Chebyshev lowpass filter prototype g_0 and g_1 are 1.0 and 0.2. Using (11)-(15), the related parameters of two BPFs are calculated and listed as: for the 50%-FBW filter, $L_1 = 390$ pH, $L_2 = 155$ pH, $L_3 = 410$ pH, $C_1 = 106$ fF, $C_2 = 77$ fF, and $C_3 = 166$ fF; for the 110%-FBW filter, $L_1 = 940$ pH, $L_2 = 255$ pH, $L_3 = 236$ pH, $C_1 = 700$ fF, $C_2 = 37$ fF, and $C_3 = 283$ fF. It is seen from Fig. 5 that two broadband BPFs with 110% FBW (from 12 GHz to 42 GHz) and 50% FBW (from 19 GHz to 31 GHz) at developed. Both two designs have the same return-loss level at -20 dB, and two TZs located at two edges, which sharp the selectivity of passband. It is noted that due to the low value of Q_{ex}, the extra resonant pole ω_2' is relatively low (smaller than -20 dB), which is not considered as a harmonic mode and thus will not affect the performance of two filters.

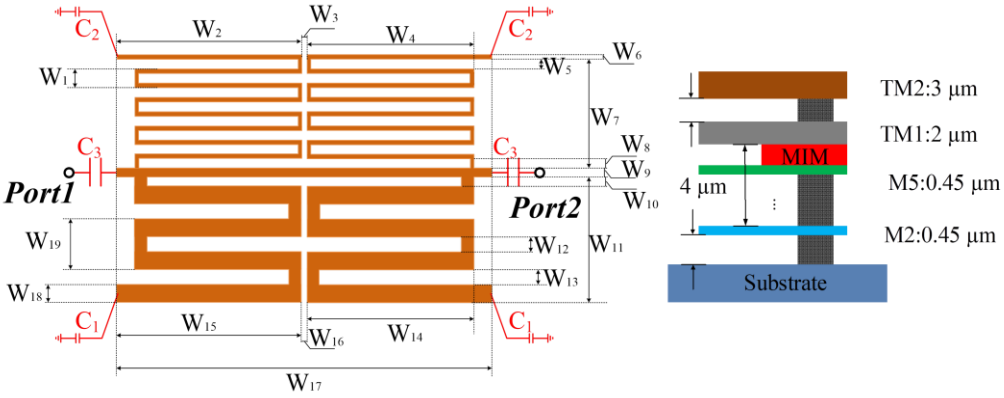

Fig. 7. The top-view of the designed BPF with selected metal stack-up for implementation. Note: W_1 = 30 μm, W_2 = 190 μm, W_3 = 4 μm, W_4 = 170 μm, W_5 = 22 μm, W_6 = 4 μm, W_7 = 192 μm, W_8 = 16 μm, W_9 = 11.6 μm, W_{10} = 11 μm, W_{11} = 103 μm, W_{12} = 12 μm, W_{13} = 12 μm, W_{14} = 170 μm, W_{15} = 190 μm, W_{16} = 4 μm, W_{17} = 384 μm, W_{18} = 14 μm, and W_{19} = 40 μm.

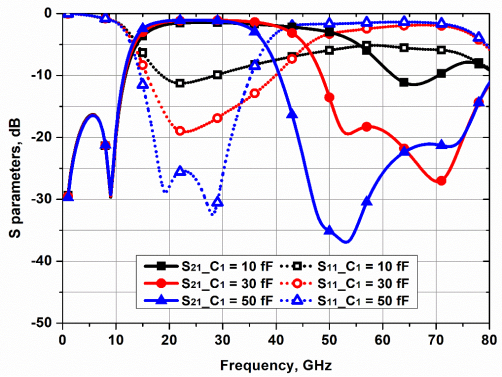

Fig. 8. EM simulated S_{21} of the designed BPF, while C_1 is swept from 10 fF to 50 fF with a step of 20 fF, C_2 = 0.4 pF and C_3 = 0.4 pF.

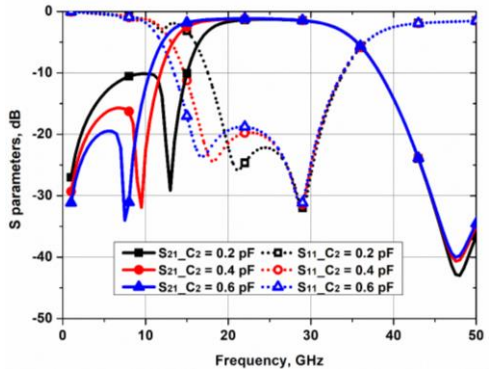

Fig. 9. EM simulated S_{21} of the designed BPF, while C_2 is swept from 0.2 pF to 0.6 pF with a step of 0.2 pF, C_1 = 30 fF and C_3 = 0.4 pF.

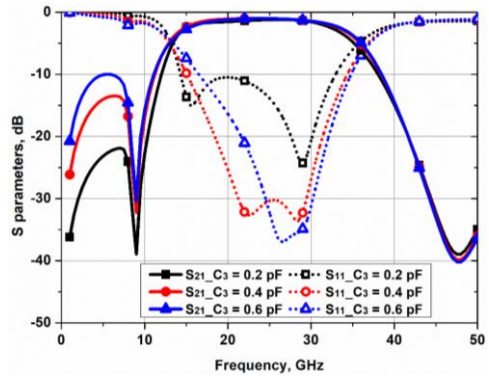

Fig. 10. EM simulated S_{21} of the designed BPF, while C_3 is swept from 0.2 pF to 0.6 pF with a step of 0.2 pF, C_1 = 30 fF and C_2 = 0.4 pF.

III. Implementation of Broadband BPFs Using Si-based Technology

A. Design Flow for BPFs

In this work, broadband BPFs are targeted to be realized using Si-based technology with constant passband and multiple TZs. Before implementing the design in EM environment, a design flow is given in this section in order to verify the presented simplified circuit model in the previous section is correct and useful to guide the design and implementation of BPFs. There are five steps to complete the design, which are summarized in Fig. 6.

In Step 1, the values of capacitance and inductances of the lumped components need to be determined using the presented simplified equivalent circuit model in Fig. 2. For a design with specified filtering characteristics, such as FBW, in-band ripple level, TZs, values of lumped components should be chosen properly. It is noted that there may be more than one optimized solution for the selection of values, which is indicated in the previously provided theoretical analysis. Thus, multiple design iterations might be required to obtain the optimized results in practice. Understanding of the principle behind the presented structure could help to optimize the design efficiently.

Once the values of all lumped components are initialized, in Step 2, the length and width of each metal line representing the inductance in Fig. 2 can be approximately estimated using the following equation:

$$L = 0.2 \ln\left(\frac{2(h+\frac{t}{2})\pi}{w+t}\right) \text{ nH/mm} \qquad (16)$$

where h is the distance from the edge of the wire to the ground ring, w and t are the width and thickness of metal strip. As far as design miniaturization is concerned, the most critical part to be designed is the low-frequency TZ. Using a combination of small inductance and large capacitance is desirable, as the large capacitance can be implemented by metal-insulator-metal (MIM) technology.

In Step 3, the pre-selected inductors can be folded accordingly based on a given die area. It is noted that although both spiral and meander line structures can be used to implement folded inductors, the meander line structure is preferred due to a higher self-resource frequency. This is particularly true as a relatively large inductance value needs to be implemented for realization of the low-frequency TZ.

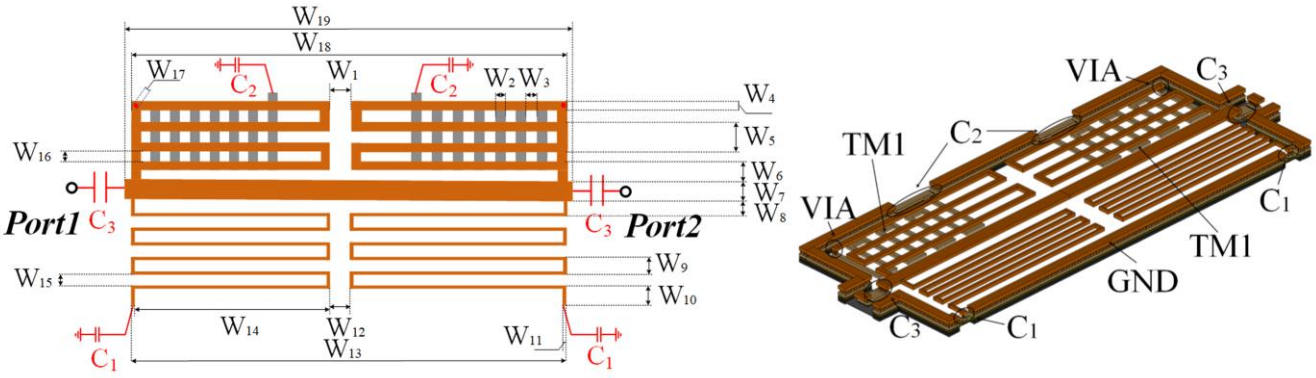

Fig. 11. The top-view as well as the 3-D view of the 2nd BPF. Note: W_1 = 20 μm, W_2 = 4 μm, W_3 = 12 μm, W_4 = 4 μm, W_5 = 20 μm, W_6 = 15 μm, W_7 = 11.6 μm,

In Step 4, based on the determined folding pattern for inductors as well as the pre-selected capacitance values, the overall performance of the BPF can be further optimized. As a rule of thumb, once the length of metal strip is fixed, changing the width of metal strip has an impact on the value of inductance. Increasing the width of a metal strip results in a reduced inductance. Changing the values of inductances can be used as a course tuning, while for a fine tuning the values of capacitance can be varied.

After the optimization is completed, the designed performance will be compared with the design specifications. If the design specifications are not satisfied, then another design iteration will be required to start from the Step 3 again. This optimization process only involves fine tuning of the length and width of the metal lines and capacitance values in EM environment, which will be discussed in the following sections. Once all required design specifications are obtained, the design will end and be ready for fabrication.

B. *Implementation of the 1st BPF*

Using the presented design flow above, a BPF is designed and implemented in a standard 0.13-μm (Bi)-CMOS technology in this Section. The top-view of BPF and the metal stack-up used for implementation is shown in Fig. 7. As illustrated, the metal stack-up provides 7 metal layers with aluminum as the thick top two metal layers. The additional MIM layer is placed between TM1 and M5. In addition, the height of the silicon substrate is 200 μm. The dielectric constant of SiO_2 is 4.1 and the loss tangent is 0.01.

Moreover, four meander lines are used in the design to form the required inductance values, while additional six MIM capacitors are used for fine tuning of the frequency responses. The top two and bottom two meander lines are used to represent the inductance L_2 and L_1 shown in Fig. 2, respectively. To implement the required inductance values, the initial ratio for the number of fingers used for top and bottom meander lines is set to be 2. Using (16) the inductance values can be further optimized. To achieve a relatively large inductance, not only using several metal fingers is required, but also needs to have a minimized metal width, which is indicated from (16). In contrast, a relatively small inductance can be implemented using a wider metal strip. Using the above-mentioned analysis along with a full-wave EM simulator, the BPF shown in Fig. 7 is designed and implemented. The frequency responses of the BPF with different capacitance values for C_1 are given in Fig. 8. As can be seen, the high-frequency TZ of the filter is shifted to a lower frequency, while a larger capacitance value is used. The impact on frequency responses using different capacitance values for C_2 and C_3 is also investigated. The results are given in Figs. 9 and 10, respectively. It is noted that the inductance values can also be used for fine tuning, but it might significantly change the die area. Therefore, it is desirable to fix the values of inductance based on a given area then carefully optimizing the frequency responses of the BPF by tuning the values of capacitors.

C. *Implementation of the 2nd BPF*

Although excellent frequency responses of the 1st BPF has been achieved, it is desirable to further reduce the physical dimensions of the BPF from an on-chip implementation point of view. For this reason, a miniaturized design example is given in this Section, in which the metal strips are folded vertically to reduce die area. The top-view as well as the 3-D view of the 2nd design is shown in Fig. 11.

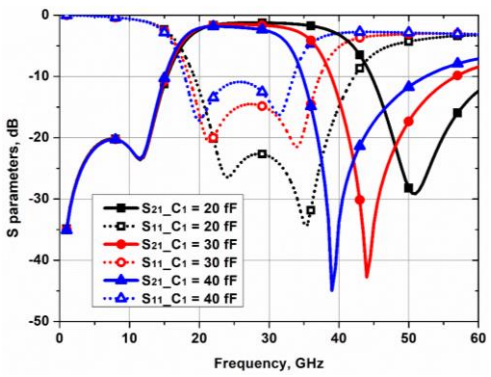

Fig. 12. EM simulated S_{21} of the designed BPF, while C_1 is swept from 20 fF to 40 fF with a step of 10 fF, C_2 = 0.4 pF and C_3 = 0.2 pF.

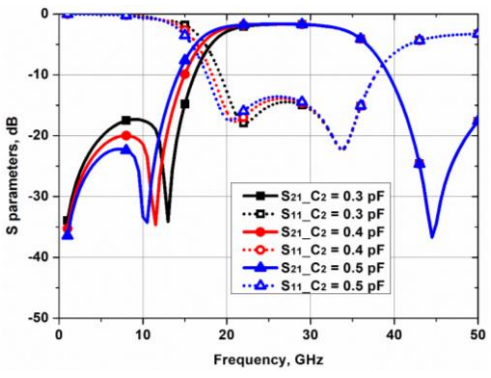

Fig. 13. EM simulated S_{21} of the designed BPF, while C_2 is swept from 0.3 pF to 0.5 pF with a step of 0.1 pF, C_1 = 30 fF and C_3 = 0.2 pF.

TABLE I
PERFORMANCE SUMMARY OF THE DESIGNED BPFS WITH THE OTHER STATE-OF-THE-ART DESIGNS

REF.	*fc* (GHz)	Insertion loss (dB)	FBW (%)	Stopband suppression @ high side (dB)	Stopband suppression @ low side (dB)	Area (mm^2)	Area (λ_g^2)
[2]	11.6	3.2	18.1	36	35	0.475	0.003
[3]	25	2.5	31	38	50	0.28	0.008
[4]	64	4.9	18.8	55	30	0.5	0.094
[5]	60	9.3	10	n/a	n/a	0.11	0.018
[6]	35	4.5	37.8	48	n/a	0.124	0.007
[7]	65	3.4	18.5	30	35	0.074	0.014
[8]	60	4.1	17	50	50	0.287	0.047
[9]	60	4	27.6	35	27	0.16	0.026
[10]	31	2.4	22.6	20	n/a	0.024	0.001
[11]	60	2.5	21	18	15	0.156	0.03
[12]	33	2.6	18	44	n/a	0.031	0.002
[13]	34	2.6	41	n/a	n/a	0.038	0.002
[14]	59.5	3.3	21.7	30	18	0.054	0.009
1ST DESIGN	**23**	**2.3**	**78.3**	**23**	**32**	**0.148**	**0.004**
2ND DESIGN	**26.6**	**2.6**	**70**	**45**	**32**	**0.066**	**0.002**

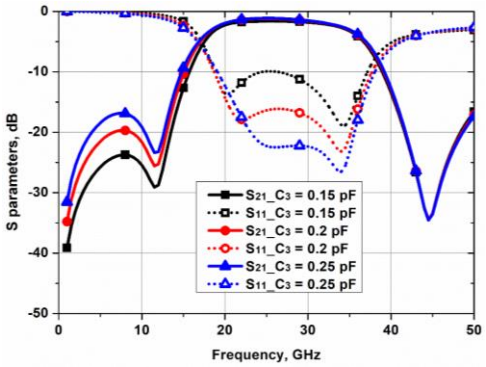

Fig. 14. EM simulated S_{21} of the designed BPF, while C_3 is swept from 0.15 pF to 0.25 pF with a step of 50 fF, C_1 = 30 fF and C_2 = 0.4 pF.

As shown, unlike the 1st design that is a planar structure, this design utilizes a lower metal layer, namely TM1, to obtain the required inductance values without increasing area. The folded metal strips in TM1 are connected with the top metal layer TM2 through VIAs. The frequency responses of the 2nd BPF with different capacitance values for C_1 are given in Fig. 12. As can be seen, the high-frequency TZ of this filter is shifted to a lower frequency, while a larger capacitance value is used. This is very well matched with the simulation results presented in Fig. 8. The impact on frequency responses using different capacitance values for C_2 and C_3 is also investigated. The results are given in Figs. 13 and 14, respectively. Both are shown reasonable agreement with the ones presented in Figs. 9 and 10, respectively, which once again indicates that the previously presented analysis is correct and useful for assisting BPF design.

IV. EXPERIMENT AND MEASUREMENT RESULTS

Two BPF prototypes are fabricated in a standard 0.13-µm (Bi)-CMOS technology. Excluding the pads, the chip sizes of the 1st design is only 0.37 × 0.4 mm^2, while the 2nd design is even smaller, 0.26 × 0.4 mm^2. Using a vector network analyzer (VNA), N5245A PNA-X, from Keysight, the S-parameters of the BPFs are measured up to 50 GHz via on-wafer G-S-G probing. Measurements were made by using conventional short-load-open-thru (SLOT) on-wafer calibration to move the reference planes from the connectors of the equipment to the tips of the RF probes.

Both the EM simulated and measured S_{21} and S_{11} of the 1st BPF are plotted in Fig. 15. As illustrated, the return loss is better than 10 dB from 13.5 to 32 GHz, which indicates a FBW of more than 78%. In addition, the minimum insertion loss of 2.3 dB is achieved within the frequency range from 17 GHz to 27 GHz and the in-band magnitude ripple is less than 0.1 dB. Thus, a reasonable agreement between the EM simulation and measurements on the 1st BPF is obtained. The discrepancy between the EM simulated results and measured data in the passband is mainly because the G-S-G probing pads were not involved in EM simulation. For the 2nd design, the physical dimensions of the filter are dramatically reduced by vertically folding metal strips using a lower metal layer. Both the EM simulated, and measured results are presented in Fig. 16. As illustrated, the return loss is better than 10 dB from 17.3 to 35.9 GHz, which indicates a FBW of more than 70%. In addition, the minimum insertion loss of 2.6 dB is achieved within the frequency range from 21.4 GHz to 27.7 GHz and the in-band magnitude ripple is less than 0.1 dB.

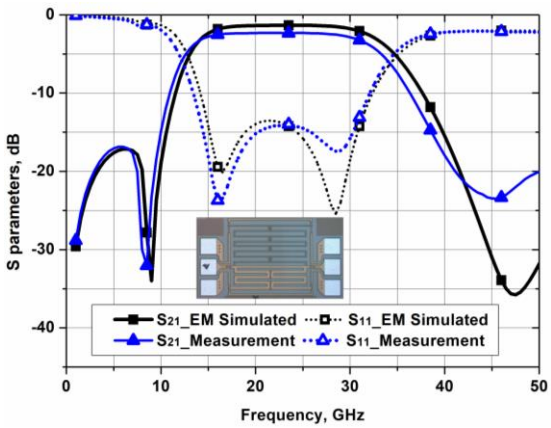

Fig. 15. Comparisons between EM simulated and measured results of the 1st design.

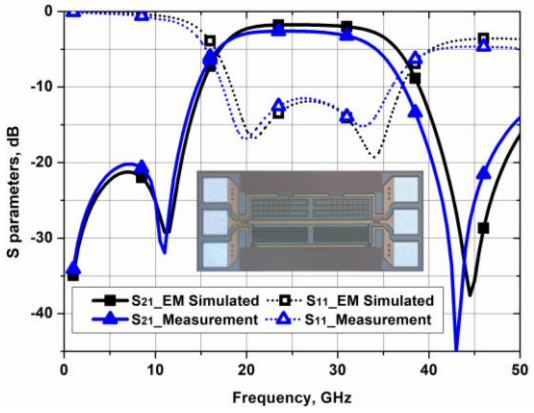

Fig. 16. Comparisons between EM simulated and measured results of the 2nd design.

For comparison purpose, the performance of the designed BPFs is summarized in Table I, where the performance of the other state-of-the-art designs are also given. Since different BPFs are designed for different specifications, it is difficult to provide an apple-to-apple comparison. However, based on the summarized results, the presented BPFs are perhaps the only solution that can be found in the literature to provide *FBW* of more than 70% with good stopband suppression and passband flatness at mm-wave region.

V. Conclusion

In this work, a methodology that can be used for on-chip BPF design with ultra-broadband is presented. To show the principle of this method, a simplified *LC*-equivalent circuit model is given and used for analysis. Using the result as a design guideline, the performance of BPF can be further optimized using a full-wave EM simulator. Finally, two BPFs are implemented and fabricated in a standard 0.13-µm (Bi)-CMOS technology. Reasonable agreements between the EM simulated and measured results are obtained. The measured results of the 1st design shows that the return loss is better than 10 dB from 13.5 to 32 GHz, which indicates an FBW of more than 78%. In addition, the minimum insertion loss of 2.3 dB is achieved within the frequency range from 17 GHz to 27 GHz and the in-band magnitude ripple is less than 0.1 dB. The chip size, excluding the pads, is only 0.148 mm^2. To demonstrate the possibility for design miniaturization, the 2nd design is given. Its physical dimensions are dramatically reduced by vertically folding metal strips using a lower metal layer. The return loss is better than 10 dB from 17.3 to 35.9 GHz, which indicates a FBW of more than 70%. In addition, the minimum insertion loss of 2.6 dB is achieved within the frequency range from 21.4 GHz to 27.7 GHz and the in-band magnitude ripple is less than 0.1 dB. The chip size for this design, excluding the pads, is only 0.066 mm^2 (0.164 × 0.4 mm^2). Based on the achieved results, it can be concluded that the presented quasi-lumped component approach is very well suitable for on-chip ultra-broadband BPF design operating at microwave and millimeter-wave region.

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