Automatic Number Plate Recognition System on an ARM-DSP and FPGA Heterogeneous SoC Platforms

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Sponsored by EPSRC and CitySync[3] (A wholly owned subsidiary of Image Sensing Systems[4], Inc.)

Introduction

The arithmetic capability of digital signal processors (DSPs), the multiple peripheral interfaces and the high frequency execution of the ARM processors make them an attractive choice for real time embedded systems. DSPs are already widely used for applications such as audio and speech processing, image and video processing, and wireless signal processing. Practical applications include surveillance, video encoding and decoding, and object tracking and detection in images and video. On the other hand, rapid development of Field Programmable Gate Arrays (FPGAs) offers alternative way to provide a low cost acceleration for computationally intensive tasks such as digital signal processing. Most of these applications use ARM, DSPs and FPGAs due to the processing power offered, in order to provide portability and real-time capability, and create custom embedded architectures for different application requirements. The main goal of this work is to design and implement efficient and novel architectures for automatic number plate recognition (ANPR) system using ARM-DSP System-on-Chip platform, which operates in high definition (HD) and in real time. In addition, a separate ANPR algorithm is developed and optimised, by taking advantage of technical features of FPGAs which accelerate digital image processing algorithms. The investigation of the algorithm and its optimisation focused on real time image and video processing for license plate (LP) or number plate localisation (NPL), LP character segmentation (NPS) and optical character recognition (OCR) in particular, which are the three key stages of the ANPR process [1]. ANPR often forms part of an intelligent transportation systems. Its applications include identifying vehicles by their number plates for policing, control access and toll collection.

ANPR system on an ARM-DSP

This complete system, is an embedded standalone, intelligent and capable of capturing and processing license plates on board the device, and represents an advance on the traditional commercial ANPR system which uses a standard definition camera to capture the vehicles, with a separate nearby computer to process the images. The major advantages of the embedded system presented here include a reduction in cost and increased portability, as the system no longer requires separate processing hardware and expensive multiple data transferring media. The algorithm developed for the ANPR system is optimised for the multicore DM8168 Chip from Texas Instruments, which contains ARM CORTEX - A8 (1.2 GHz) and C674x DSP (1 GHz) which is a floating-point Very-Long-Instruction-Word (VLIW) DSP. The optimisation is achieved through the efficient use of internal and external device memory with different resources utilised depending on its suitability for the algorithm used, in order to achieve real time processing. In addition, we have taken advantage of the HD video processing subsystem on the device to facilitate full HD video capture (1920 X 1080), encoding and decoding. The video frames are then transferred to the ARM side of the Chip for processing; which is where communication with the DSP is established. The overall system operates at 14 frames per second and with over 95% recognition success using a large (70K plus) UK and European database of LP images. The ANPR algorithms developed are advanced work based on earlier research work using fixed point DSPs published by the authors in [2], [3] and [4].

ANPR on FPGA

The second part of the investigation focused on developing and accelerating a full ANPR algorithm on FPGA. A range of image processing algorithms and architectures for each ANPR stage (i.e. NPL, NPS and OCR) have been developed and optimised to exploit features and innovations available within new FPGAs [5][6][7]. The proposed architectures have been implemented and verified using the Mentor Graphics RC240 FPGA development board equipped with a 4M Gates Xilinx Virtex-4 LX40. The ANPR full algorithm takes less than 10 ms and consumes only 80% of the FPGA on-chip resources. The overall results achieved show that the entire ANPR algorithm can be implemented on a single FPGA that can be placed within an ANPR camera housing to create a stand-alone unit.

Conclusion

The ARM-DSP based ANPR system described is designed for commercial applications where the need for low power, low prices and real time systems is vital. A single FPGA can also be added as a "plug-in" to the ARM-DSP based hardware SoC, depending on the extra resources needed for the application. The overall results have shown that it is possible to use cheaper off-the-shelf ARM-DSPs and FPGAs multicore processors for "standalone" ANPR systems through device and algorithm optimisation to achieve real-time performance at higher recognition rate using efficient algorithms.

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[1]University of Essex, [2]Qatar University.
[3]CitySync, "ANPR Company," http://www.citysync.co.uk/go.php/en/home/home.html.
[4]Image Sensing Systems, "Intelligent Transportation Systems Company" http://www.imagesensing.com/company.html.

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- Automatic Number Plate Recognition (ANPR) systems are used to track, identify and monitor moving vehicles by automatically extracting their number plates

Current ANPR systems

- Require high performance workstations and expensive computers for real-time processing
- Use a separate camera and a separate computer for data processing
- Cost, compactness, and power consumption issues

Proposed FPGA based ANPR system

- A full ANPR algorithm on an FPGA - 4M Gates Xilinx Virtex-4 LX40
- Can be integrated within an ANPR camera
- Parallelism and pipelining can be exploited to meet the real-time requirements
- Removing the need for the installation and cabling costs, Low power consumption

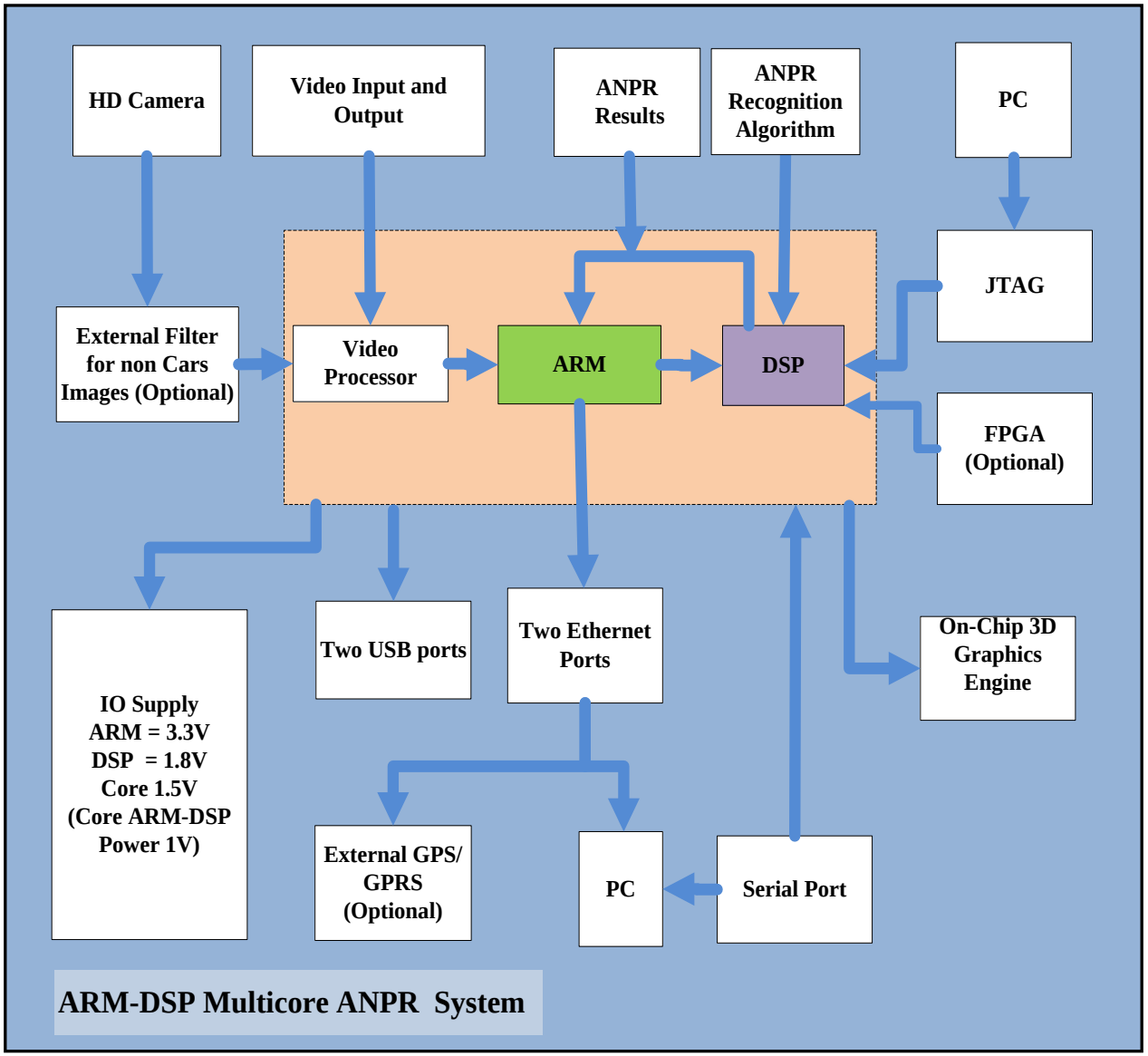
Proposed ANPR system based on ARM-DSP multicore SoC

- A complete “standalone” and embedded ANPR system operating in real time and using full HD images (1920 X 1080) at lower cost
- Using DM8168 Chip and EVM from Texas Instruments containing ARM CORTEX – A8 (1.2 GHz) and C674x DSP (1 GHz) which is a floating-point Very-Long-Instruction-Word (VLIW) DSP

Software utilisation on the ARM-DSP heterogeneous device

- LP detection on a DSP is based on a robust and comparative study of edge detection method, connected component analysis (CCA) and histogram analysis (HA).
- This is followed by an efficient DSP based LP character segmentation algorithm, which uses wavelet transform along with CCA and HA.
- ARM based Character Recognition is performed using neural networks.
- Algorithms are tested using a large (70K+) UK and European database of images.

A Complete ANPR System on an ARM-DSP Heterogeneous SoC Platform

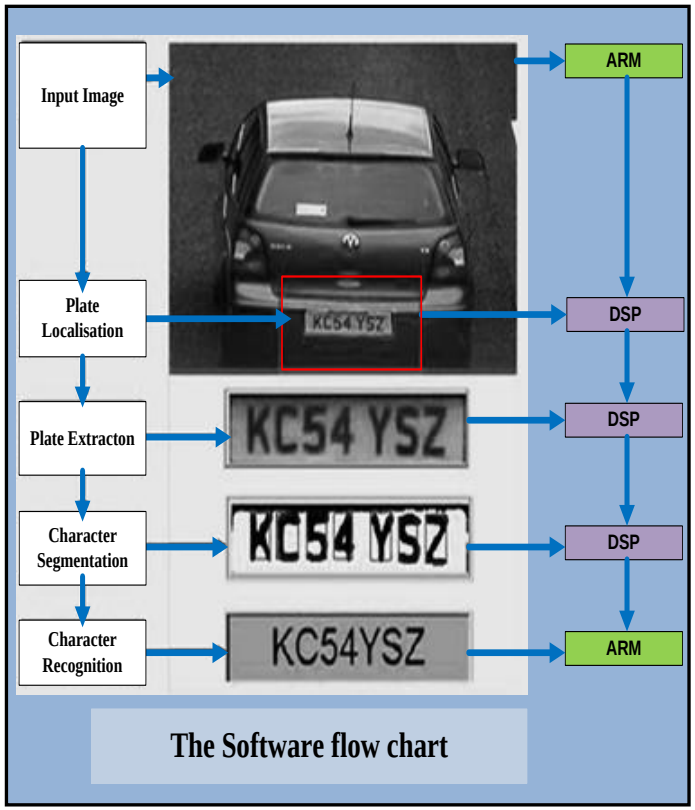


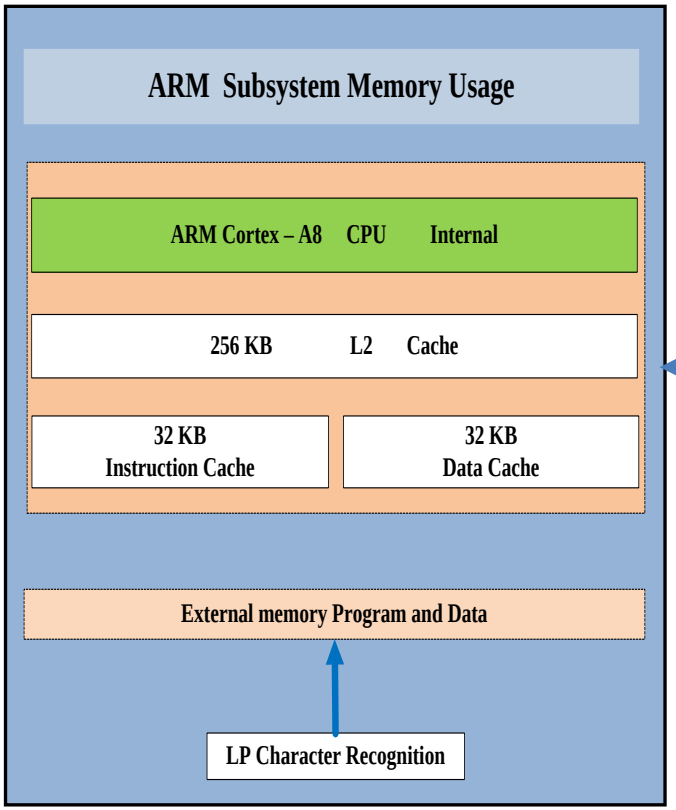
- ARM is a 32-bit RISC processor includes 32 KB of Instruction Cache, 32 KB of data Cache, 256 KB of L2 Cache
- The C674x floating-point DSP processor uses 32KB of L1 program memory and 32KB of L1 data memory and 256 KB of L2 RAM

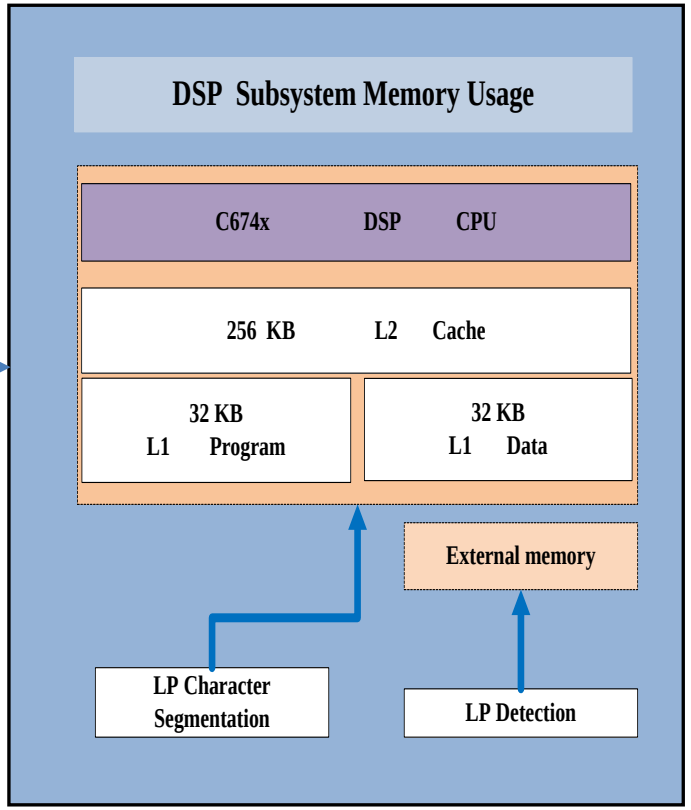
DSP Optimisation Techniques

- Data Cache Optimisation Source Code optimisation by moving large data from L2 RAM to external memory
- Linear assembly programming for Optimisation of instruction latencies
- Software pipelining – parallelism

ARM-DSP ANPR System Software Memory Utilisation

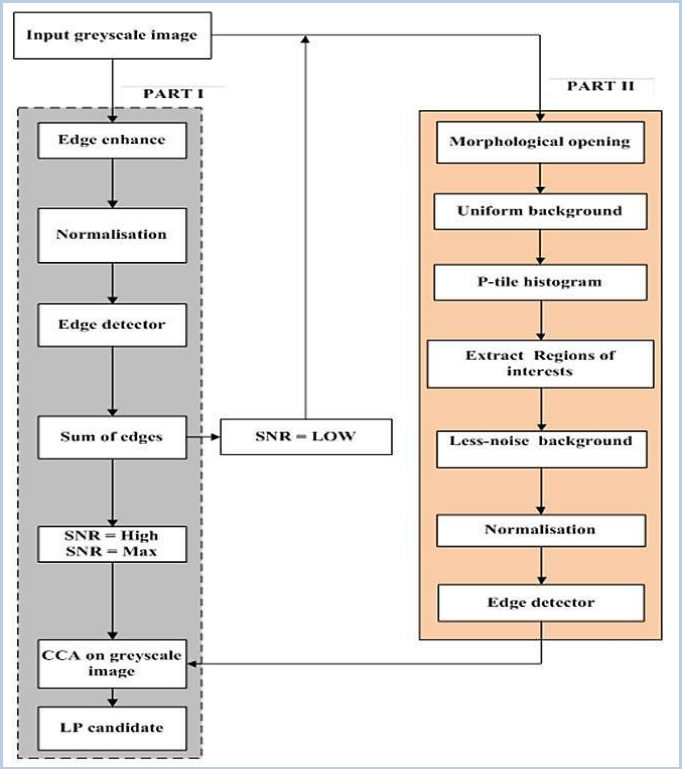


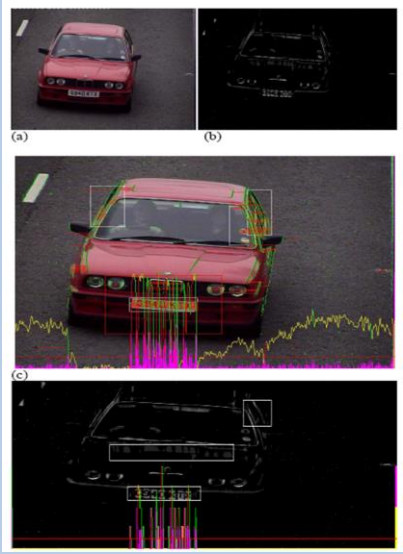




- LP localisation and detection is performed on the External Memory of the DSP, due to the size of the data
- To speed up the process, LP Character Segmentation is performed on the internal RAM of the DSP.
- Character recognition is also performed on the ARM of the system, for ease of maintenance but can equally run on DSP efficiently
- The Chip has dual 32-Bit DDR2 (800) and DDR3 (1600) (External memory up to 4 GB)

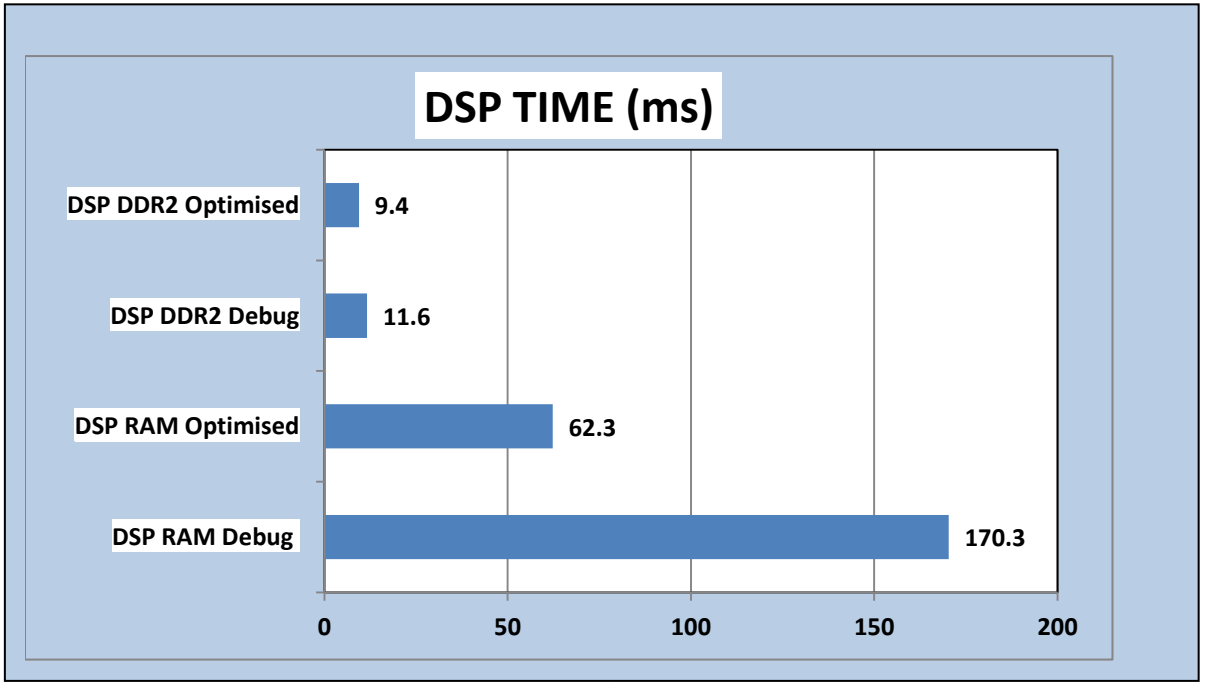
Performance of LP detection Algorithm on DSP





(a) Input image
(b) Morphological opening on (a)
(c) Histogram analysis of (a)
(d) Histogram analysis using of (b) and extracted LP confirmed in a white box using connected component analysis with high histogram response in both (c) and (d)

- Signal-to-Noise Ratio (SNR) is defined by the ratio of an original image to a processed image through their differences using:
  - Sum of edges of images with high success detection and
  - Sum of the edges in the test processed image



- The LP detection algorithm is firstly executed using RAM. The performance was slow due to the size of the image (1920 x 1080) data
- Faster time is achieved by moving the entire image data to the external memory

LP Segmentation Algorithm on DSP

ALGORITHM LISTING: LP character segmentation based on 2D Haar WT

- *Let $f(x, y)$ be an input image*
- *For each wavelet decomposition level j = 1…N*
- *Compute DWT coefficients at level j based on Haar WT*
- *End*
- *Let $d_{HV}(x, y)$ be the horizontal and vertical coefficients at final level N*
- *Compute the reconstruction of $d_{HV}(x, y)$ using IDWT (See Figure 2)*
- *Let $E_{HV}(x, y)$ be the result from reconstruction*
- *Compute the absolute value*
- *Let $E_{ABS}(x, y)$ be the absolute edges*
- *Compute the prominent edges through optimal threshold T*
- *Let E_{Haar} be the prominent 2D Haar WT edges*
- *Compute contrast comparison on $f(x, y)$ to find edges*
- *Let E_{CON} be initial edges by contrast comparison*
- *Compare E_{CON} to E_{Haar} to confirm edges*
- *Let E_{FIN} be the final edges*
- *Compute connected component analysis on the final edges*
- *Let CCA be the connected components*
- *Compute histogram analysis on CCA to confirm characters*
- *Let HA be the histogram analysis results*
- *Compute bounding box around character*

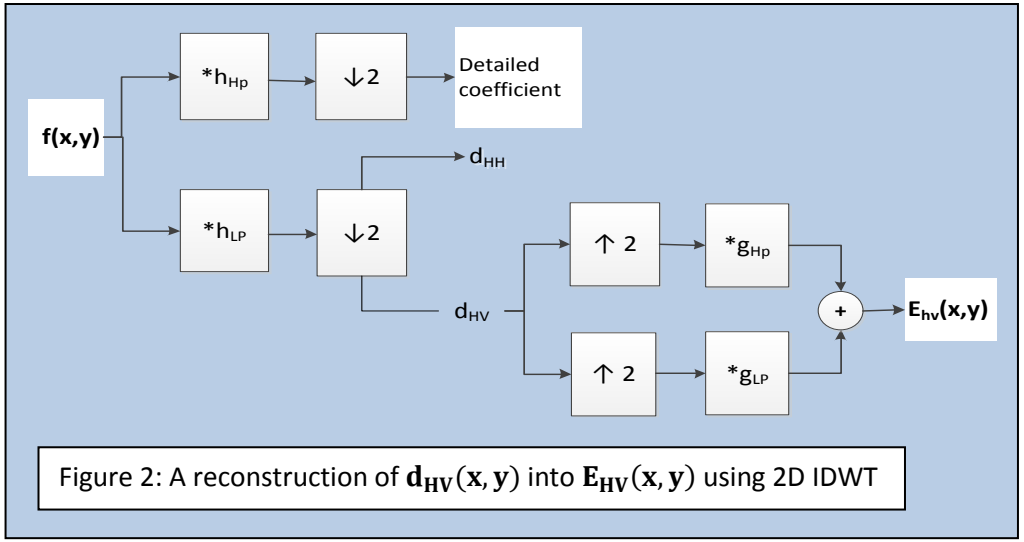
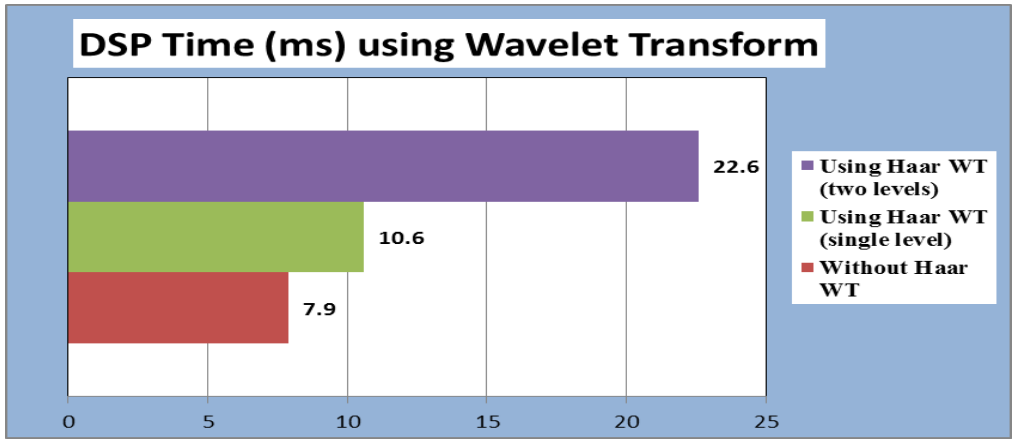
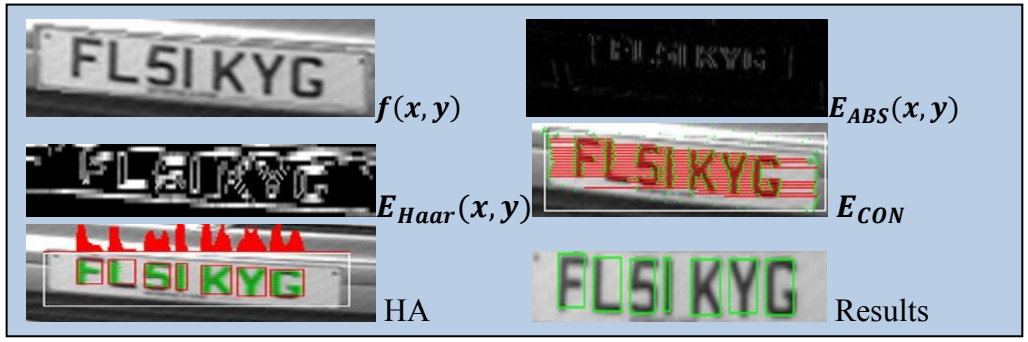


Figure 2: A reconstruction of $\mathbf{d_{HV}(x, y)}$ into $\mathbf{E_{HV}(x, y)}$ using 2D IDWT





Block diagrams of proposed ANPR solution on FPGA

Input Image

Number Plate Localisation (NPL) Module

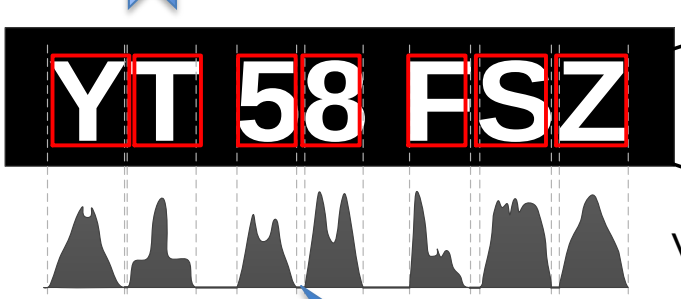
Pre-processing Module

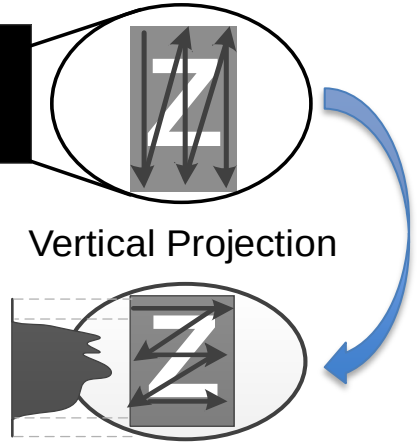
Character Segmentation (CS) Module

Optical Character Recognition (OCR)

YT 58 FSZ

Recognised Characters





Vertical Projection

Horizontal Projection

Original RGB Images

Greyscale Images

Morphological Open

Background Images

Filtered Image

Morphological *Open*

Binarised Image

Thresholding

Highlighted Plate Region

Morphological Close

Connected Component Analysis (CCA) on binary image

Fully Connected Plate Region

Number Plate

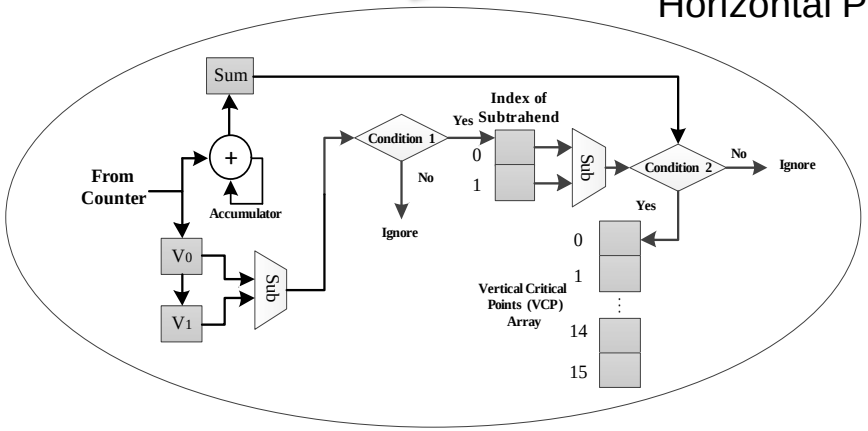
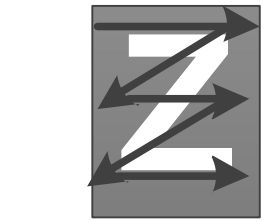


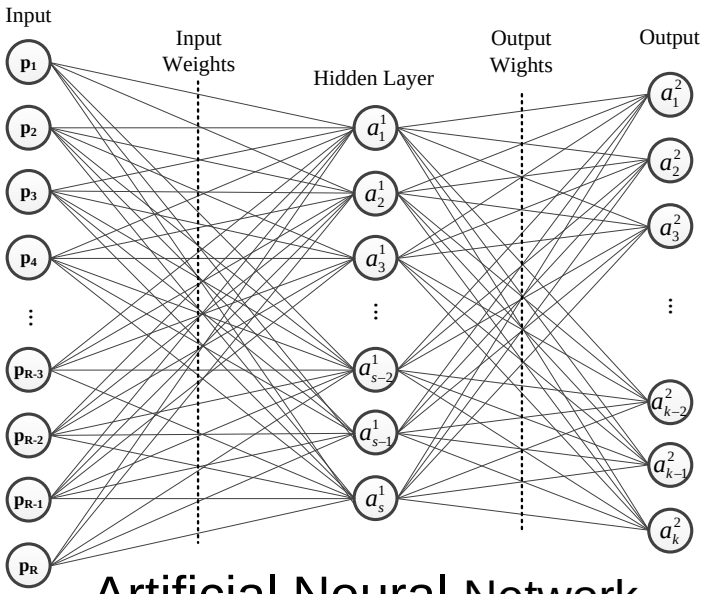
Plate Feature Extraction Part

Selection of Candidates Plate Region

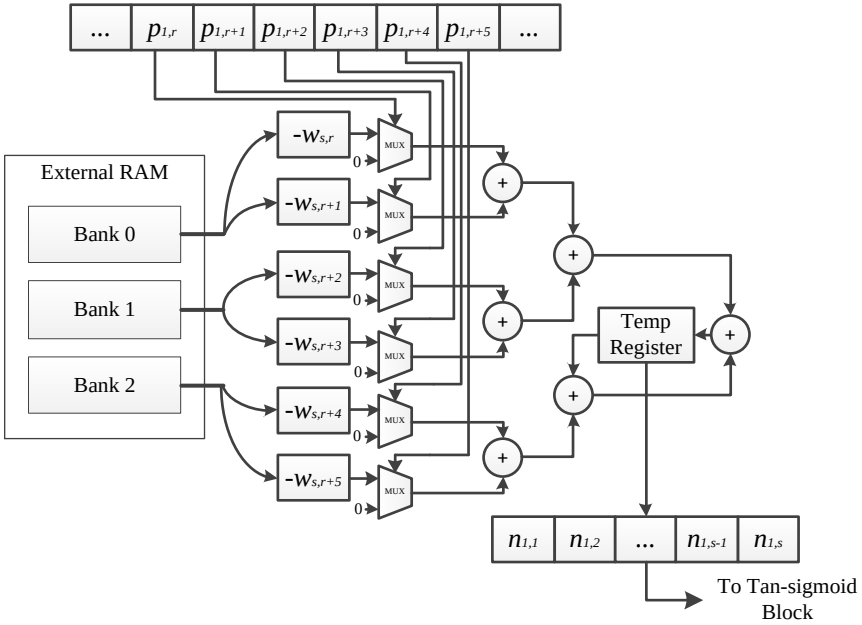
Block diagrams of proposed ANPR solution: OCR

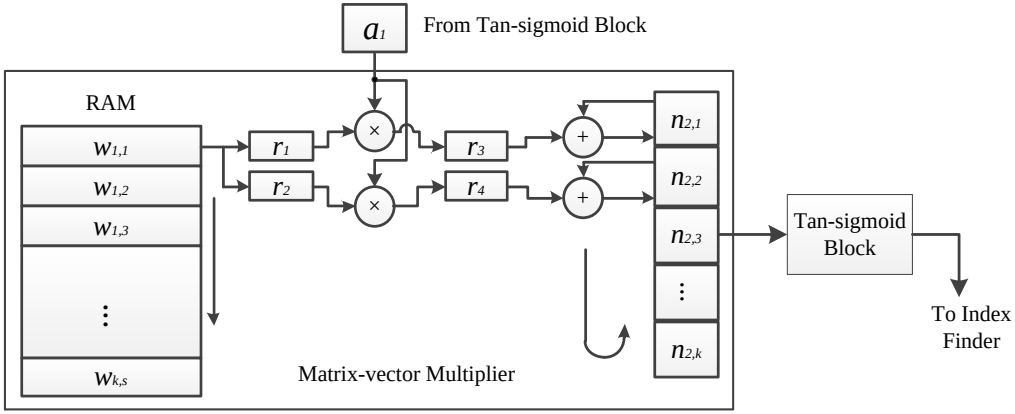


Character Image



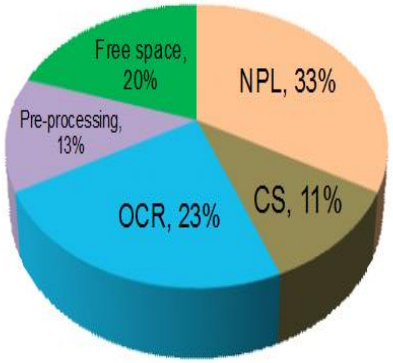
Encoded Text





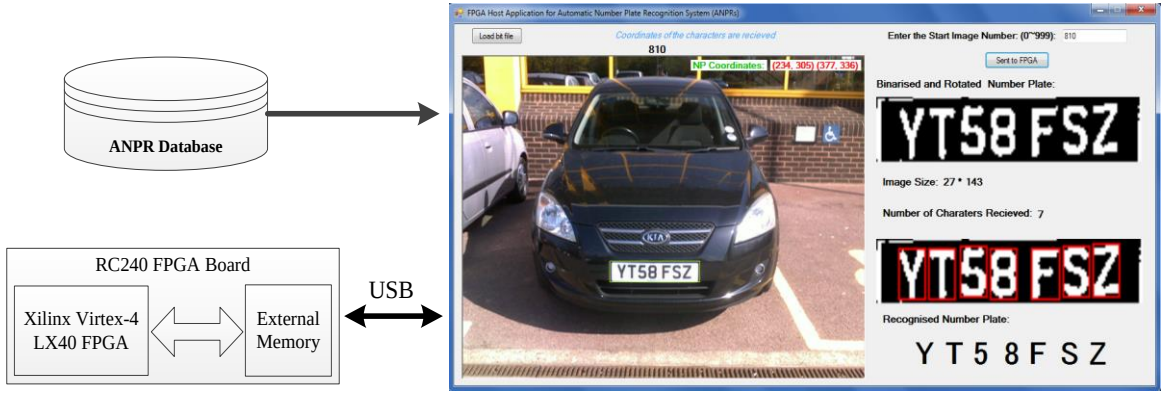
Results achieved

- Improved low complexity NPL, CS, OCR, pre-processing algorithms and their novel efficient architectures have been designed and successfully implemented on a 4M Gates Xilinx Virtex-4 LX40 FPGA
- Tested using 5570 SD (640 X 480) images achieving real time processing under 10 ms using 80% of FPGA resources



FPGA resource usage

ANPR Stages	Used Algorithms	Speed (ms)	Successful Rate (%)
NPL	Morphological operation and CCA	4.7	97.8
CS	Morphological operation	0.2-1.4	97.7
OCR	Two layers feed-forward Neural network	0.7	97.3
Pre-processing	Local threshold and nearest neighbour interpolation	0.11	N/A



Host application used for graphically viewing the results from FPGA

Results on an ARM-DSP SoC platform

- The complete system proposed on an ARM-DSP SoC platform used a number of complex algorithms including Wavelet transform, Morphological operations and Neural network to improve ANPR algorithms and speed.
- Conclusively, DSP computes algorithms faster and real time is achieved through optimisation. The ANPR performance is under 20 ms, which is real time
- Tested using over 70K images and 95% plus success rate achieved
- The overall system on ARM-DSP is operating at 14 frames per second using full HD video (1920 X 1080).

Results on FPGA

- The overall results achieved show that the entire ANPR algorithm can be implemented on a single FPGA. FPGAs can also be used to offload extra processing as a plug-in to ANPR camera system such as the ARM-DSP described to create a standalone unit.
- The benefits of standalone and all-in-one embedded ANPR system proposed are the reduction in overall cost