A CMOS 750MHz Fifth-Order Continuous-Time Linear Phase Lowpass Filter with Gain Boost

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***Abstract*– The design and implementation of a CMOS continuous-time multiple loop feedback (MLF) leap frog (LF) filter is described. The filter is implemented using a fully–differential linear, low voltage operational transconductance amplifier (OTA). PSpice simulations using a standard TSMC 0.18μm CMOS process with 1.8V power supply have shown that the cut-off frequency of the filter ranges from 455MHz to 780MHz and dynamic range is about 58dB. The group delay is less than 5% over the whole tuning range; the maximum power consumption of the filter with gain boost is only 240mW.**

I. INTRODUCTION

Linear phase lowpass filters have been widely used for hard disk drive (HDD) read channels to equalize the input signals. Among different filter structures, the cascade structure has attracted the most attention [1, 2]. However, the cascade structure has higher sensitivity, compared with multiple loop feedback (MLF) structures. Therefore, research has been conducted on HDD read channels by using MLF structures recently [3-6]. The inverse-follow-the-leader-feedback (IFLF), follow-the-leader-feedback (FLF) and leap frog (LF) structures all have been used for equalizers design. However, none of them can exceed the cut-off frequency of 500MHz. The HDD systems are high performance systems and near real-time applications [7], which continue to develop at a rapid and deterministic pace to meet the emerging demands of high performance computing and peripheral devices. Moreover, the industry is seeking for the solutions for next generation HDD systems, whose data rates can be up to 2Gb/s. We need a filter whose cut-off frequency is at least 700MHz; however, it is a challenge to design a filter at such ultra high frequency using pure CMOS. On the other hand, power consumption needs to be even lower, because more and more digital systems are expected to be integrated on the single chip due to using advanced deep submicron process. The easiest way to reduce the power consumption is reducing the power supply voltage. However, most specifications of a filter rely on the supply voltage strongly. Alternatively, we need to reduce the filter order to fulfill the overall power consumption requirement. In this paper, our design is targeted at a MLF LF linear phase filter for HDD read channels, which can work at cut-off frequency of 750MHz with accurate linear phase, gain boost, and low power consumption.

The design of a fully-balanced OTA is discussed in Section II. Filter architecture and synthesis are described in Section III. The simulation results are given in Section IV, and finally conclusions are given in Section V.

II. FULLY–BALANCED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Source degeneration OTAs have received more attention than any other techniques based OTA due to the tradeoff between linearity and power consumption. However, it has to pay the expense of the reduced overall transconductance. Moreover, the tuning range of the source degeneration OTA relies strongly on the triode region transistors, and thus it is relatively small [1, 5]. An alternative OTA is presented in this section to optimize the linearity and power consumption, which is shown in Figure 1.

DC Response of the OTA

The CMOS OTA in Figure 1 is used for the filter design.

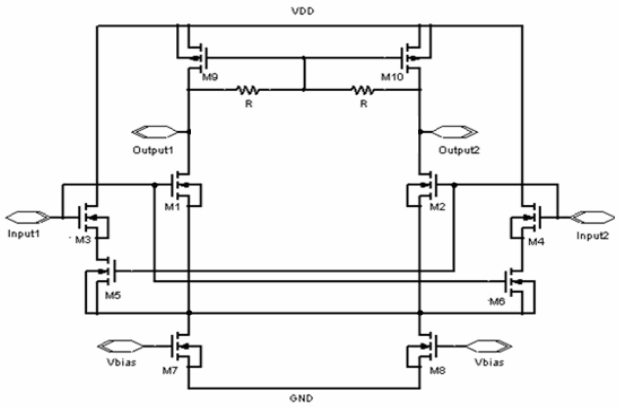

Figure 1 Fully-balanced OTA

In this unit OTA cell, M_1 and M_2 are the input transistors. M_3–M_6 act as active biasing circuitry in such a way that the total current drawn by M_3–M_6 is required for larger signals. The active biasing shares the same bias current source with the differential pair M_1 and M_2. When the signal amplitude is small, M_3 and M_4 are in saturation while M_5 and M_6 are in triode region. The M_3–M_6 branches remove some of the bias current. When the signal amplitude is positive and large, M_6 will become saturated and M_5 will be cut off. A smaller proportion of the total bias current will be drawn by M_3–M_6. This results in larger currents in M_1 and M_2 to compensate for the drop of the transconductance. The sizing of the transistors must be optimized for maximum linearity [8]. The analysis starts from I_{D3} and I_{D5}:

$$\begin{aligned} I_{D3} &= I_{D5} \\ &= X \cdot K_3\left(\frac{V_{in}}{2} - V_{d5} - V_T\right) \\ &= 2K_5\left[-\left(\frac{V_{in}}{2} + V_{cm} + V_T\right)\cdot V_{ds5} - \frac{1}{2}V_{ds5}^2\right] \end{aligned} \tag{1}$$

Let $V_{cm}+V_T=V_{cm}'$, $K_{3,4}$ is X times $K_{5,6}$ then I_{D3} can be expressed as:

$$I_{D3} = K_3\left[\frac{V_{in}}{2} - (V_{ds5} + V_{cm}')\right]^2$$

$$= \frac{K_3}{4(X+1)^2}\left[2V_{in} - \sqrt{(1-3X)V_{in}^2 + 4(X+1)V_{in}V_{cm}' + 4(X+1)V_{cm}'^2}\right]^2 \tag{2}$$

I_{D4} has a similar expression, with V_{in} replaced by $-V_{in}$. Therefore, the output current is then given by

$$I_{out} = K_{1,2}\sqrt{\frac{I_B - \left[\frac{K_{1,2}}{2} - \frac{K_{3,4}}{2(X+1)^2}(5-3X-4\sqrt{X+1})\right]V_{in}^2}{2[K_{1,2}+(X+1)K_{3,4}]}}V_{in} \tag{3}$$

Using Taylor series, then equation (3) can be expanded as follows,

$$I_{out} \approx \sqrt{\frac{K_{1,2}^2 I_B}{2[K_{1,2}+(X+1)K_{3,4}]}}V_{in} - \frac{K_{1,2}^2 - \frac{K_{1,2}\cdot K_{3,4}}{(X+1)^2}(3X+4\sqrt{X+1}-5)}{12\sqrt{[K_{1,2}+(X+1)K_{3,4}]\cdot 2I_B}}V_{in}^3 \tag{4}$$

Note that the even order harmonic distortions are ideally zero due to the symmetry of fully differential OTA. The total harmonic distortion (THD) is mainly determined by the third harmonic distortion (HD3). We may have a complete HD3 cancellation as long as the following condition is met,

$$K_{1,2}^2 = \frac{K_{1,2}\cdot K_{3,4}}{(X+1)^2}(3X + 4\sqrt{X+1} - 5) \tag{5}$$

The above equation gives us an insight into how to design the OTA meeting the specification of linearity. Therefore, the transconductance of OTA can be expressed as,

$$g_m \approx \sqrt{\frac{K_{1,2}^2 I_B}{2[K_{1,2}+(X+1)K_{3,4}]}} \tag{6}$$

Second-order Effects of the OTA

Second-order effects, such as mobility reduction, body effect causing deviations from the ideal square-law behavior of MOS devices have been neglected in the above analysis. However, high frequency filters require the use of high electric fields, thus the mobility reduction effects must also be taken into account. As a first order approximation, mobility reduction in MOS transistors may be modeled as,

$$\mu = \frac{\mu_0}{1+\theta(V_{gs}-V_T)} \tag{7}$$

Where μ_0 is the zero-field mobility of carriers, θ equals to $1/(T_{ox}E_{CR})$ is the coefficient of the effect of the electric field on the mobility, T_{ox} is the gate oxide thickness and E_{CR} is the critical field. On the other hand, the dependence on the bulk-source voltage resulting in body effect is another potential cause of nonlinear behavior in the voltage-to-current conversion of the OTA in Figure 1. If the transistors are not connected to V_{DD} or ground, the bulk-source voltages V_{BS} are not equal to zero and the threshold voltage can be expressed as,

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right) \tag{8}$$

Where V_{T0} is the threshold voltage for V_{BS} equal to zero, γ is the bulk threshold parameter, and ϕ is the strong-inversion surface potential. Including equation (7) and equation (8), equation (6) can be approximated by equation (9),

$$g_m' \approx \sqrt{\frac{K_{1,2}I_B}{2\left[\frac{(X+1)^3}{4\sqrt{X+1}+3X-5}\cdot\frac{1+\theta(V_{gs1,2}-V_{T1,2})}{1+\theta(V_{gs3,4}-V_{T3,4})}+1\right]\cdot[1+\theta(V_{gs1,2}-V_{T1,2})]}} \tag{9}$$

Thus, the mobility reduction limits the transconductance of the OTA.

Frequency Response of the OTA

Owing to the absence of internal nodes, the OTA in Figure 1 has excellent high-frequency performance. Figure 2 shows the small-signal model of the equivalent half-circuit of the OTA in Figure 1 with capacitive loads for frequency analysis. Using this model, the voltage transfer function of the OTA-C integrator can be shown as

$$A_v(s) = \frac{V_{out}(s)}{V_{id}(s)} = \frac{g_m}{s(C_L + C_p) + G_{out}} \tag{10}$$

Where C_L and C_p are the load capacitance and parasitic output capacitance of the OTA, respectively, and G_{out} is the OTA's output conductance. The two parameters: C_p and G_{out} of the model are given by

$$C_p = C_{DS1} + C_{DS11} + C_{GD1} + C_{GD11}$$
$$G_{out} = g_{o1} + g_{o11} \quad (11)$$

Where g_{oi} is the output conductance of the MOS transistors of the OTA.

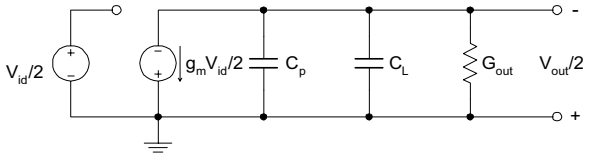

Figure 2 Small signal model of Figure1 with capacitive loads

From equation (10), the differential open-loop DC gain of the OTA can be obtained as

$$A_{v0} = \frac{g_m}{G_{out}} \quad (12)$$

Equation (12) reveals that the OTA in Figure 1 does not have very high DC gain. We may see that the DC gain of the OTA can be increased by increasing either g_m or reducing G_{out}. g_m can be increased by increasing the W/L ratios of the input transistors. However, the DC drain currents of the input transistors are also increased proportionally, thus resulting in increased output conductance of the input transistors. Consequently, no significant increase in DC gain is expected. Moreover, the power consumption is increased as the W/L ratios are increased. Fortunately, the lowpass filter for HDD read channels are low Q applications; moderate DC gain is enough to adjust the Q location. The OTA's bandwidth (BW) is determined by its dominant pole, which is located at the output nodes (as the highest impedance occurs at these nodes) and is approximately given by

$$BW \approx f_d \approx \frac{G_{out}}{2\pi(C_L + C_p)} \quad (13)$$

Where f_d is the dominant pole frequency of the OTA. Thus, the open-loop gain-bandwidth product of the OTA is the multiplication of equations (12) and (13)

$$GBW = \frac{g_m}{2\pi(C_L + C_p)} \quad (14)$$

Note that BW can be written as a function of GBW as

$$BW = \frac{GBW}{A_{v0}} \quad (15)$$

It is crucial to note that there is a tradeoff between BW and A_{v0} as can be seen from equation (15). In other words, high bandwidth can be obtained at the expense of reduced DC gain and vice versa.

III. FILTER ARCHITECTURE AND SYNTHESIS

The normalized characteristic of a fifth–order lowpass 0.05° equiripple linear phase filter with real zeros at the cut-off frequency is given by:

$$H_d(s) = \frac{(s^2 - 1)}{D(s)} \quad (16)$$

With

$$D(s) = 0.201926s^5 + 0.822285s^4 + 2.075924s^3 + 3.033116s^2 + 2.604527s + 1$$

The fully balanced realization of the function in equation (16) using the current–mode LF structure with output summation OTAs is shown in Figure 3.

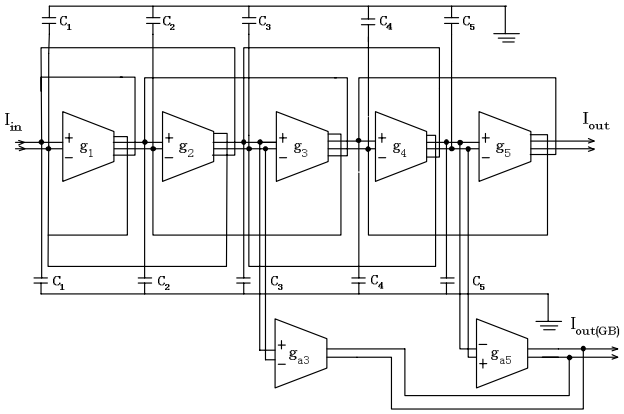

Figure 3 Fifth–order LF OTA–C filter with output summation OTA network

The overall transfer function of the circuit can be derived as

$$H(s) = \frac{I_{out(GB)}}{I_{in}} = \frac{N(s)}{D(s)} \quad (17)$$

Where

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_2\tau_3\tau_4\tau_5 s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_4\tau_5 + \tau_3\tau_4\tau_5)s^3 + (\tau_2\tau_3 + \tau_2\tau_5 + \tau_4\tau_5)s^2 + (\tau_1 + \tau_3 + \tau_5)s + 1$$
$$N(s) = \alpha_3\tau_4\tau_5 s^2 + (\alpha_3 - \alpha_5)$$

The design formulae for the filter can be attained by coefficient matching between (16) and (17) [9]. The resulting pole $\tau_i = C_i/g_i$ and zero $\alpha_i = g_{\alpha i}/g_i$ parameters are:

$$\tau_1 = 0.24557, \tau_2 = 0.61776, \tau_3 = 0.84468, \tau_4 = 1.04066, \tau_5 = 1.51427, \alpha_3 = 0.36544, \alpha_5 = 0.63456 \quad (18)$$

The filter is designed with identical unit OTAs using the CMOS OTA cell in Figure 1 to improve OTA matching and facilitate design automation. The cut-off frequency of the filter is chosen around 600 MHz. Using the computed parameter values in equation (18) and choosing identical transconductance of 14mS for g_i (i=1,2…5) the transconductances $g_{\alpha 3}$ and $g_{\alpha 5}$ can be calculated from equation (18) as 5.1mS and 8.9mS, respectively, the capacitor values can also be calculated, but the parasitic

capacitance must also be taken into account. For the circuit of Figure 1, the parasitic capacitance is about 0.2pF. The capacitance values are recalculated below:

C_1=1.0748pF, C_2=2.7038pF, C_3=3.697pF, C_4=4.5549pF, C_5=6.6276pF.

IV. Simulation Results

The circuit was designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18µm CMOS process available from MOSIS [10]. Figure 4 shows the magnitude response of the filter with and without gain boost. As can be seen from Figure 4, the gain boost of the filter is about 5dB. By varying the bias voltage of the unit OTA cell, the tuning range of cut-off frequency without gain boost is 455–780MHz. The maximum total power consumption of the filter is about 240mW at 780MHz cut-off frequency for a single 1.8V power supply.

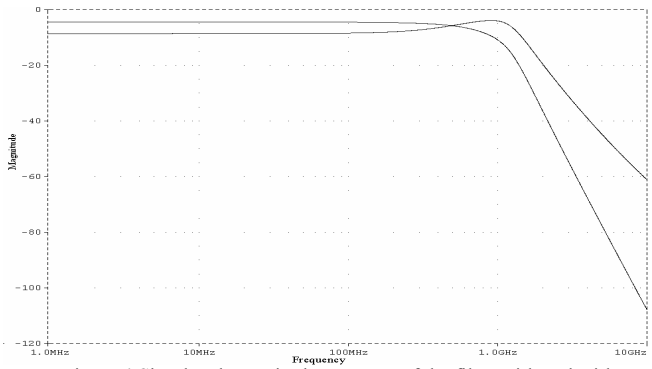

Figure 4 Simulated magnitude response of the filter with and without gain boost

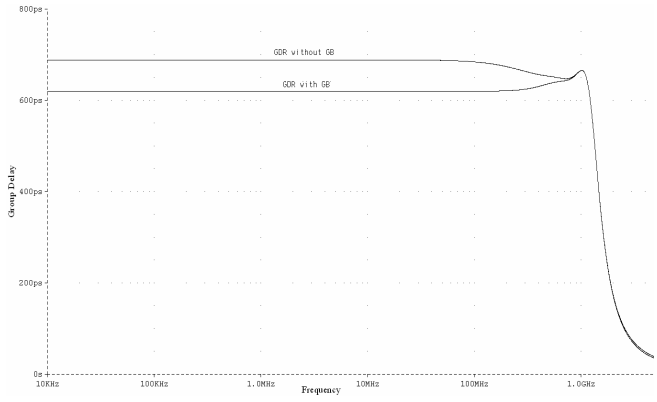

Figure 5 Simulated group delay response with and without gain boost

The filter phase response with and without gain boost are fairly linear, as can be seen from Figure 5; the group delay has very small variation up to the twice of the cut-off frequency and it is shown that the gain boost has effect on the group delay ripple of filter due to the finite DC gain of the presented OTA, but the group delay ripple is still less than 5%. The filter's group delay ripple for $0 \le f \le 1.7f_c$ is approximately 4% with the group delay ripple below ±25ps over the whole tuning range. This is well within the limit of the read channel filter specification. Simulation of the filter has shown a THD of less than 1% with a single tone of 1mA. The dynamic range is about 58dB at f_c =750MHz. The performance of the filter offers significant improvements; especially the power consumption is much smaller than other designs, making the presented filter well suitable for portable electronics products. To compare the proposed solution with previous publications, the Figure of Merit (FOM) is defined; all of the parameters such as bandwidth in MHz, geometry in µm, gain boost (GB) coefficient 1.5, and power consumption per pole in mW are taken into account.

$$FOM = \frac{GB \cdot [Bandwidth]^2 \cdot Geometry}{Power} \qquad [19]$$

The proposed filter has 3164 of FOM, which is much higher than any other MLF structures based filters in the literature.

V. Conclusions

This paper has described a 750MHz current–mode fully–balanced fifth–order linear phase lowpass filter based on the MLF LF structure, applied to a HDD read channel. A linear single stage OTA with a typically large transconductance has been used. Simulation results using 1.8V 0.18µm CMOS show that group delay ripple is around 4% with and without gain boost; the power consumption of the proposed filter is about 240mW with gain boost at f_c = 750MHz. The frequency tuning range is from 455MHz to 780MHz. These results have shown that the MLF LF filter can achieve good performance and may become one of the filtering solutions for next generation HDD systems.

VI. References

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