Low-distortion low-voltage operational transconductance amplifier

X. Zhu and Y. Sun

A new operational transconductance amplifier (OTA) is proposed, which is based on the flipped voltage follower and source degeneration techniques. The OTA is simulated in a standard TSMC 0.18 μm CMOS process with a 1.8 V supply voltage. The simulation results show that the total harmonic distortion of the proposed OTA is less than 1% up to 0.85 Vp-p.

Introduction: Recent research shows a high demand for highly linear operational transconductance amplifiers (OTAs) with an aim to reduce total harmonic distortion (THD) [1–4]. However, most of these linearisation techniques may present important drawbacks such as reduced effective transconductance and significant power consumption. On the other hand, low power supply and power consumption solutions are needed for handheld products. However, the scaling down of threshold voltage does not follow the drop in the nominal supply voltage. As the available voltage headroom becomes limited, many existing circuit techniques in the analogue domain cannot be applied. Moreover, mismatch issues are also critical owing to the use of deep sub-micro processes [5]. Consequently, the second-order harmonic distortion cannot be eliminated properly. Without focus on linearisation, the linearity of the OTA will be rather poor. Very often, large gate–source voltages are required in order to improve OTA linearity, but the supply voltages limit this benefit especially for low-voltage applications. Therefore, a new OTA is proposed in this Letter, which is based on the flipped voltage follower (FVF) [6] and source degeneration techniques. Use of source degeneration optimises the linearity and the power supply is reduced by the FVF technique.

Proposed OTA: Fig. 1 shows the new OTA configuration. The presented configuration uses a differential pair in the input stage with source degeneration. The output stages consist of four current mirrors. The tail current source is taken over by a pair of dynamic current mirrors based on the FVF structure. The input stage currents are differentially mirrored through p-type current mirrors M_{7-10} and n-type current mirrors M_{3-6} to the outputs. The transistors M_{16} and M_{17} are in the triode region, their gate voltages are connected to be biased with a control current source I_{bias} through transistors M_{11-15}. It is worth mentioning that the geometry of the input devices also affects the transconductance value, DC gain and noise. To shift the poles to higher frequencies, and obtain the large transconductance, the channel length used for these transistors is the minimum length allowed by the process. Transistors M_{16} and M_{17} could be connected either in serial or in parallel. It depends on the purpose that the OTA is used for. To optimise the power consumption, parasitic effects and high-frequency response, the triode transistors are connected in parallel. If a large tuning range is needed, they may be connected in serial. The OTA in Fig. 1 uses a serial structure as an example. The drain current of MOS transistors M_{16} and M_{17} in the triode region is given by, when $V_{DS} \ll V_{GS} - V_T$ and assuming $M_{16,\ 17}$ are identical:

$$I_R = K(V_{GS} - V_T)V_{DS} \tag{1}$$

where $K = 0.5\ \mu C_{ox}(W/L)$ is the n-type transconductance parameter, and μ, C_{ox}, W and L are mobility, oxide capacitance per unit area, channel width and length, respectively. Then:

$$I_{out} = I_{out\ 1} - I_{out\ 2} = 2\ I_R \tag{2}$$

By substituting (1) into (2) we get:

$$I_{out} = 2\ K(V_{GS} - V_T)V_{DS} \tag{3}$$

Note that $2V_{DS} \simeq V_{in}$, when source degeneration is deep. Therefore, we get:

$$I_{out} \simeq K(V_{GS} - V_T)V_{in} = g_m V_{in} \tag{4}$$

where V_{in} is the differential input voltage and g_m is the DC transconductance of the proposed OTA, given by:

$$g_m \simeq KV_B, \quad V_B = V_{GS} - V_T \tag{5}$$

From (4) and (5), we can see that the OTA exhibits a linear V − I characteristic with the assumptions made. Equation (5) shows that the transconductance value can be controlled by varying the bias voltage V_B. Thus, the allowed values of V_B determine the achievable transconductance tuning range. The bias voltage V_B can be adjusted by the bias current source I_{bias} through transistors M_{11-15} in the OTA.

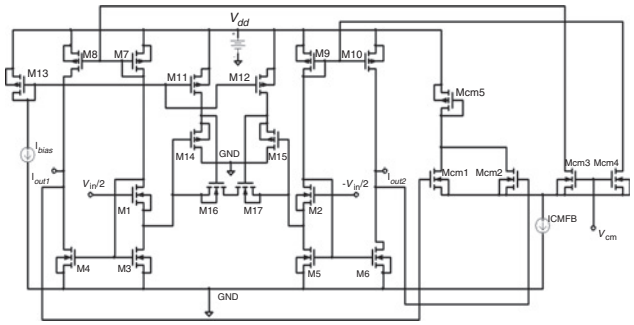

Fig. 1 *Circuit diagram of proposed OTA*

However, for high-frequency applications the second-order effects are severe, therefore often in implementation, the bulk/substrate of most transistors in Fig. 1 are tied to ground or V_{DD}, apart from the two input stage transistors $M_{1,\ 2}$. For this case, the threshold voltages of M_1, M_2 are modulated, which will result in the so-called body or threshold modulation effects. The threshold voltage of an NMOS transistor is defined by

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) \tag{6}$$

where V_{T0} is the threshold voltage with zero bias, γ is the body/bulk polarisation factor or bulk threshold parameter, ϕ is the strong inversion surface potential and V_{BS} is the voltage between bulk and source. With the mentioned threshold modulation effect for Fig. 1, using (4) the modified I_{out} can be shown as

$$I'_{out} = g'_m V_{in} \tag{7}$$

where $g'_m = K[V_{GS} - V_{T0} - \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi})]$ is the modified DC transconductance of the OTA. Hence, there is an error in g_m' caused by $\Delta V_T = \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi})$. Thus the bulk effects cause nonlinear behaviour in g_m with respect to V_{in}. In practice, thinner gate oxides are recommended to minimise the body effects as γ is decreased with a smaller oxide thickness at the expense of increased mobility reduction. The first-order model of mobility reduction or degradation in MOS transistors is given by

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)} \tag{8}$$

where μ_o is the zero-field mobility of carriers, $\theta = 1/t_{ox}E_{CR}$ is the coefficient of the effect of the electric field on the mobility, t_{ox} is the gate oxide thickness and E_{CR} is the critical field. In relation to the proposed OTA, the mobility reduction μ causes the transconductance parameter K that is μ dependent to change. This in turn also causes variation in g_m or I_{out}. It is varied from its ideal expression as given in (4). Therefore, there is a tradeoff between transistor sizes.

Common-mode feedback (CMFB) circuit: In fully differential circuits, the common-mode DC output voltages change from their stable values as a result of process, temperature and supply variations. Therefore, it is necessary to utilise a CMFB circuit to stabilise its DC output voltages. The CMFB circuit is proposed and is shown in Fig. 1. It basically consists of two differential pairs $M_{cm1,2}$ and $M_{cm3,4}$ biased by a DC current source I_{CMFB}. The common-mode DC output voltages from the OTA are sensed by the $M_{cm1,\ 2}$ pair and compared with the reference common-mode reference voltage V_{cm} in the second differential pair $M_{cm3,\ 4}$. Any difference between the levels is amplified and correction voltages are applied to the p-type current sources loading the OTA. The size of the common-mode reference should be twice that of the common-mode sensing to keep the current densities in the load devices equal. The CMFB circuit in Fig. 1 is associated with two poles, one is dominant and the other is non-dominant. The single-pole model of the common-mode feedback transconductance is expressed as:

$$g_{m\_CMFB}(jf) = \frac{g_{m\_CMFB}}{1 + jf\left(2\pi C_{p7}/g_{m7}\right)} \tag{9}$$

where the g_{m_CMFB} is the DC transconductance of transistors $M_{cm1,\ 2}$ or $M_{cm3,\ 4}$ and C_{p7} is the related parasitic capacitance at the gate of transistor M_7. The gain–bandwidth product of the common-mode loop is given below:

$$GBW_{CMFB} = \frac{g_{m\_CMFB} g_{m8}}{2\pi g_{m7} C_L} \tag{10}$$

where C_L is total output capacitance. The parasitic capacitances need also to be taken into account. To achieve stability for the common-mode loop, the non-dominant pole frequency should be higher than GBW_{CMFB}. This condition can be further expressed (assuming $g_{m7} = g_{m8}$) as:

$$\frac{g_{m7}}{C_{p7}} \geq \frac{g_{m\_CMFB}}{C_L} \tag{11}$$

Simulation results: The OTA circuit was designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18 μm 1.8 V CMOS process available from MOSIS. With identical length of 0.18 μm, the widths of the transistors used are given in Table 1. The simulated transconductance of OTA against the differential input voltage with I_{bias} of 100 μA is shown in Fig. 2. The THD performance of the proposed OTA with different bias currents is shown in Fig. 3. It can be seen that the THD is always less than 1% when the differential input voltage is below 0.85 V owing to the elimination of even-order harmonic distortions. The dynamic range of 115 dB is achieved at 0.5% THD. The total output noise is 1.3 $\mu V/\sqrt{Hz}$. The total power consumption is about 11.8 mW for 1.1 ms transconductance.

Table 1: Widths of transistors

M_1, M_2	M_3–M_{10}	M_{11},M_{12}	M_{13}–M_{15}	M_{16}, M_{17}
10 μm	100 μm	20 μm	10 μm	7 μm
M_{cm1}, M_{cm2}		M_{cm3} M_{cm4}		M_{cm5}
20 μm		40 μm		60 μm

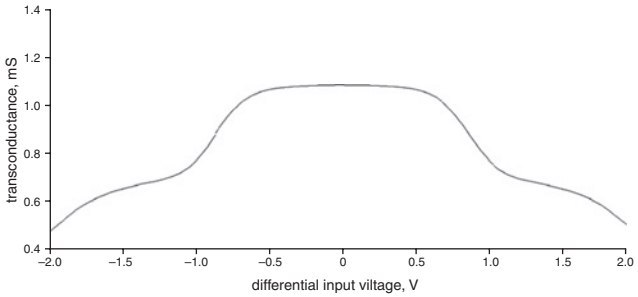

Fig. 2 *Simulated OTA transconductance against differential input voltage*

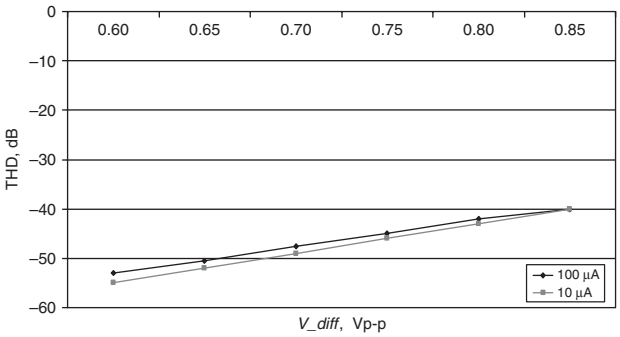

Fig. 3 *Total harmonic distortion for different bias currents*

Conclusions: A simple OTA circuit configuration achieving optimum trade-off between linearity and supply voltage is presented. It combines source degeneration and flipped voltage follower techniques. The complete OTA also contains CMFB and bias tuning circuits. Simulations in 0.18 μm CMOS show that THD of less than 1% can be achieved by the OTA for differential input voltage of up to 0.85 $V_{p\text{-}p}$ when using a 1.8 V power supply voltage. The dynamic range achieved is 115 dB with 0.5% THD. The total output noise up to 100 MHz is 1.3 $\mu V/\sqrt{Hz}$. The overall transconductance is approximately 1.1 mS. The power consumption is 11.8 mW. Therefore, the proposed OTA could be suitable for wireless communication receiver baseband applications.

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