A Field Programmable Analog Array for CMOS Continuous-Time OTA-C Filter Applications

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Abstract—A programmable high-frequency operational transconductance amplifier (OTA) is proposed and analyzed. A general configurable analog block (CAB) is presented, which consists of the proposed programmable OTA, programmable capacitor and MOSFET switches. Using the CABs, the universal tunable and field programmable analog array (FPAA) can be constructed, which can realize many signal-processing functions, including filters. A tuning circuit is also discussed. The proposed OTA has been simulated and fabricated in CMOS technology. The results show that the OTA has the transconductance tunable/programmable in a wide range of 700 times and the − 3-dB bandwidth larger than 20 MHz. A universal 5×8 CAB array has been fabricated. The chip has also been configured to realize OTA-C 60-kHz and 500-kHz bandpass filters based on ladder simulation and biquad cascade.

Index Terms—CMOS analog integrated circuits, continuous time filters, field programmable analog circuits, programmable circuits, programmable filters.

I. INTRODUCTION

IN RECENT years, field programmable analog arrays (FPAAs) have received great interest, as they can achieve benefits in analog circuit and system design as field programmable gate arrays (FPGA) have in the digital counterpart. There have been some programmable analog circuits in the literature [1]–[8], [10]–[13] as well as commercial chips (MPAA020 from Motorola [9], AN10E40 from Anadigm [31], or ispPAC family from Lattice Semiconductor Corporation [30]). However, general-purpose FPAAs suitable for high-frequency signal processing applications have not yet appeared.

Analog circuits based on the continuous-time operational transconductance amplifier and capacitor (OTA-C) technique are promising for high-frequency operation [14]–[23], [27], [28]. Having an operational transconductance amplifier (OTA) of programmable transconductance g_m and a programmable capacitor, it is possible to build filters for a wide frequency range. For most CMOS processes, it is not possible to create a capacitor with a wide range of programmability which can operate at high frequencies. Thus it is very important to have a widely programmable transconductance. The proposed OTA

has g_m that can be adjusted by a factor of 700. This results in a possibility to build filters of frequencies from several kilohertz up to several megahertz. The structure of the FPAA is composed of universal configurable analog blocks (CABs). The proposed FPAA consists of 40 CABs. A tuning circuit compensating for process variations, temperature, power supply, bias change, etc., is also considered. As examples, implementations of an *RLC* ladder-based sixth-order bandpass filter and a fourth-order cascaded biquad filter are presented.

II. CONFIGURABLE ANALOG BLOCK USING PROGRAMMABLE OTAS AND CAPACITORS

The versatile CAB consisting of one programmable fully differential OTA, one programmable capacitor C_{EQ} and a set of switches S_1–S_{12} is shown in Fig. 1. The switches are placed in such a way that the OTA can be connected with or without the capacitor. It is also possible to pass the signals of other CABs through the switches situated at the top and the bottom of the CAB. Switches S_1 and S_2 enable to connect the input to the OTA directly or in an inverse way. To program the CAB, a control word of length of 22 bits must be specified (OTA: 5 bits, capacitor: 5 bits, switches: 12 bits), as well as the voltage V_{ctrl} controlling the transconductance of the OTA. The control word is stored in a shift register, while voltage V_{ctrl} is supplied from the external automatic tuning circuit. The chip area of the CAB is 626 μm $\times$ 750 μm. FPAA circuits can be constructed using CABs to perform various functions including filtering, examples of which will be shown in Section VI.

III. PROGRAMMABLE OTA

A. Basic Principle and Structure

The simplified schematic diagram of the OTA based on two cross-coupled differential MOS pairs [16] and digitally programmable current mirrors is shown in Fig. 2. Using the standard square-law model for MOS devices, currents I_{in1} and I_{in2} defined in Fig. 2 are

$$I_{in1} = K(V_P - V_{Tp})^2 + K(V_Q - V_b - V_{Tp})^2 \qquad (1)$$

$$I_{in2} = K(V_Q - V_{Tp})^2 + K(V_P - V_b - V_{Tp})^2 \qquad (2)$$

where $K = 0.5\mu C_{ox} W/L$ is the transconductance parameter of transistors $M1$–$M4$, having the same W/L ratios, V_{Tp} is the threshold voltage, V_b is the voltage of the floating dc source, and V_P and V_Q are the gate–source voltages of transistors $M1$ and $M2$, respectively. All undefined parameters have their usual meanings.
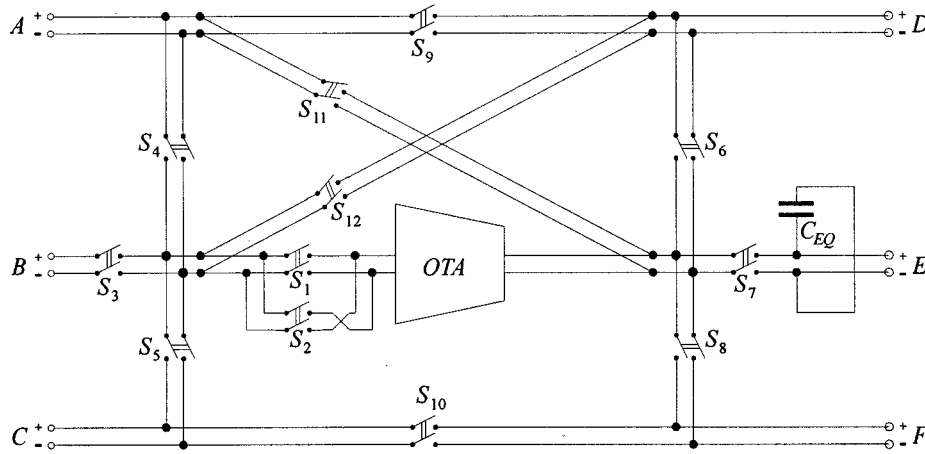
Fig. 1.   Structure of CAB. The polarity of OTAs input signal can be straight or inverse, depending on the settings of switches S_1 and S_2, respectively.
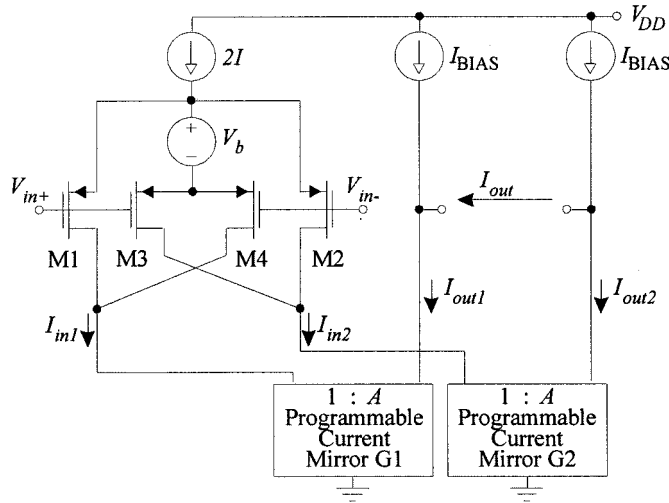

Fig. 2.   Simplified schematic diagram of the CMOS programmable OTA.

With (1) and (2), the difference between currents I_{in1} and I_{in2} can be expressed as

$$I_{\text{in1}} - I_{\text{in2}} = 2K(V_P - V_Q)V_b = 2K(V_{\text{in+}} - V_{\text{in-}})V_b$$
$$= 2KV_bV_{\text{id}} \tag{3}$$

where $V_{\text{id}} = V_P - V_Q$ is the differential input voltage. Assuming that the current gains of the programmable current mirrors all are equal to A, the output current can be derived as

$$I_{\text{out}} = \frac{1}{2}A(I_{\text{in1}} - I_{\text{in2}}) = K(V_{\text{in+}} - V_{\text{in-}})V_bA$$
$$= KV_bAV_{\text{id}} \tag{4}$$

and the overall transconductance g_m of the OTA circuit in Fig. 2 is then obtained from (4), given by

$$g_m = \frac{dI_{\text{out}}}{dV_{\text{id}}} = KV_bA. \tag{5}$$

In order to obtain a wide range of application frequencies in OTA-C filter design, it is necessary that the transconductance of

the OTA should be adjustable in a wide range. From (5) it can be seen that two methods can be used to change the transconductance g_m. One method is to tune the floating bias voltage V_b by an analog voltage. The other is to make the gain A of the output current mirrors programmable in a digital way.

B. Programmable Current Mirror Array

A current mirror of programmable gain can be realized using the well-known high compliance current mirror structure with 31 identical output stages (Fig. 3). The output current I_{out} is a sum of the currents flowing through individual output stages. As can be seen from Fig. 3, the output stages are connected in 5 groups of 1, 2, 4, 8, and 16 stages that can be simultaneously switched ON or OFF by appropriate switch S_i where $i = \{1, 2, 4, 8, 16\}$. Using n stages, the output current I_{out} can be set to the value from $I_{\text{out}}^{\text{min}} = I_{\text{in}}$ to $I_{\text{out}}^{\text{max}} = nI_{\text{in}}$ with resolution $\Delta I_{\text{out}} = I_{\text{in}}$. Only five output groups (5 bits) were implemented due to the huge area of the MOS devices of the most significant bits.

In practice, every switch S_i must be accompanied by another switch $\overline{S_i}$, which can short-circuit the gate of the transistor M_{ia} to ground. This is necessary for discharging the parasitic capacitance C_{gs} of the transistor M_{ia} and stopping the current I_i flowing. The cascoded current mirror structure is used to achieve high output resistance.

C. Complete OTA Circuit

The complete circuit diagram of the OTA is shown in Fig. 4. Transistors $M1$–$M4$ comprise the cross-coupled differential input pair, biased by the current coming from the current source (transistors $Mi1$, $Mi2$) flowing through the floating voltage V_b. Both the current source and the voltage source are controlled by voltage V_{ctrl}, so that simultaneous change of the bias current and voltage V_b with voltage V_{ctrl} is made possible. The relation between V_b and V_{ctrl} is linear.

A fully differential programmable current mirror is composed of two programmable current mirror arrays $G1$ and $G2$ (see Fig. 4). The current mirrors are based on the circuit from Fig. 3 with some modifications and consist of transistors $M5a$–d with $M7a,b$ and $M6a$–d with $M8a,b$. The current gain A of the
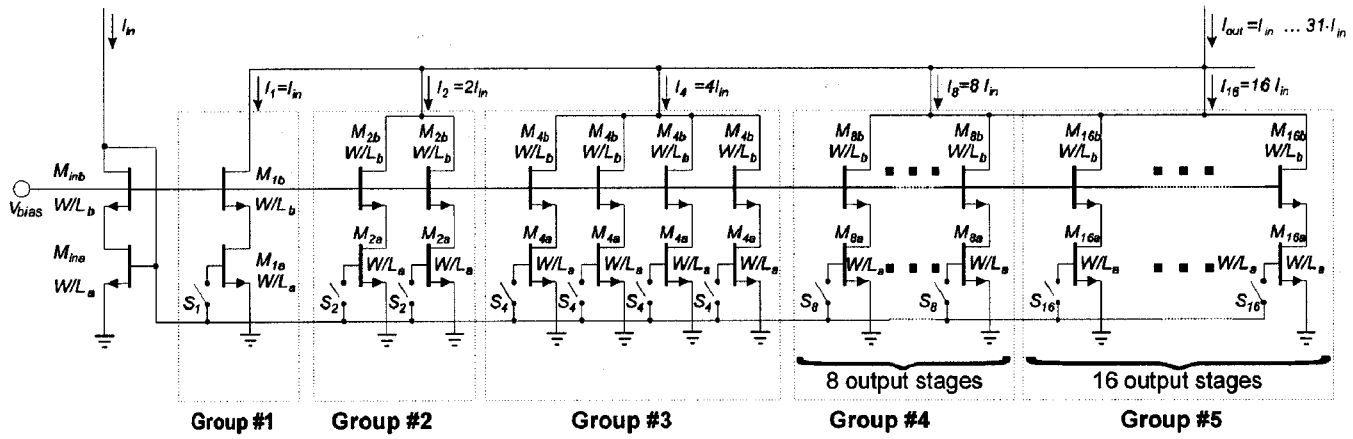
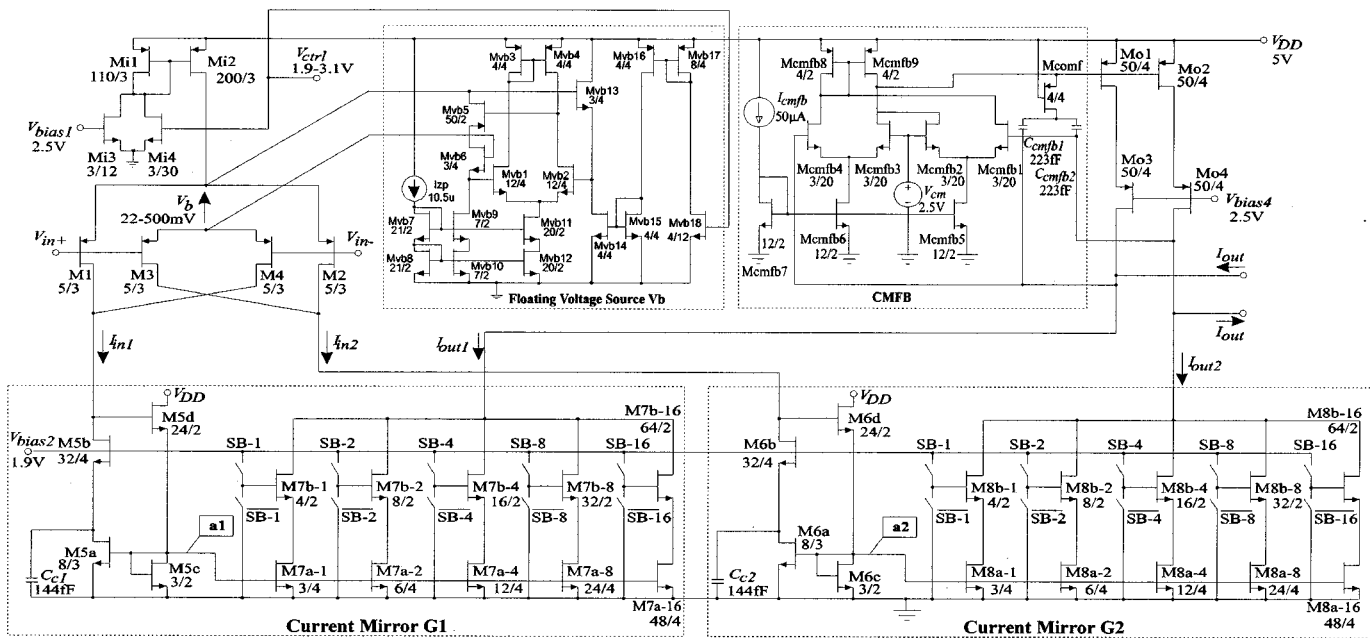Fig. 3. Simplified schematic diagram of programmable current mirror.

Fig. 4. Complete circuit diagram of the CMOS programmable OTA.

current mirror can be set very precisely by switching ON or OFF the appropriate output stages, so the transconductance g_m of the whole OTA can also be changed very accurately.

As can be seen from Fig. 4, at nodes **a1** and **a2** a significant grounded capacitance is attached, which is C_{gs} of transistors $M7a$-1 to $M7a$-16 and $M8a$-1 to $M8a$-16, respectively. In order to drive the capacitor, the buffers consisting of transistors $M5c$, $M5d$ and $M6c$, $M6d$ have been used [26]. The buffers work with a negative feedback loop (transistors $M5d$ and $M6d$), which provides very low resistance at nodes **a1** and **a2**. The capacitors C_{c1} and C_{c2} are used for frequency compensation.

To avoid further increase of the capacitance at nodes **a1** and **a2**, the switches programming the output stages are connected to the gates of transistors $M7b$-1 to $M7b$-16 and $M8b$-1 to $M8b$-16 rather than to the gates of transistors $M7a$-1 to $M7a$-16 and $M8a$-1 to $M8a$-16. Another advantage of this is the almost constant capacitance at nodes **a1** and **a2**, independent of the number of output branches switched ON.

The common mode feedback circuit (CMFB) block is responsible for regulating the average output voltage to a fixed dc voltage of 2.5 V. The CMFB circuit (transistors Mcmfb1–Mcmfb10) drives the output current source (transistors Mo1–Mo4). This current source consists of two cascoded transistors to obtain high output resistance.

To additionally increase the OTAs output resistance, voltage V_b and the current of the current source consisting of transistors Mi1 and Mi2 may be reduced. Reducing the current flowing through the output stage increases OTAs output resistance due to the channel length modulation effect. But care must be taken that such reduction will decrease the linear transconductance range.

Decreasing the voltage V_b by lowering the control voltage V_{ctrl} causes also a decrease of the constant current of the current source Mi1–Mi2. The reduction of the current flowing through transistors Mi1 and Mi2 results in reducing the current flowing through output stages, what increases their output
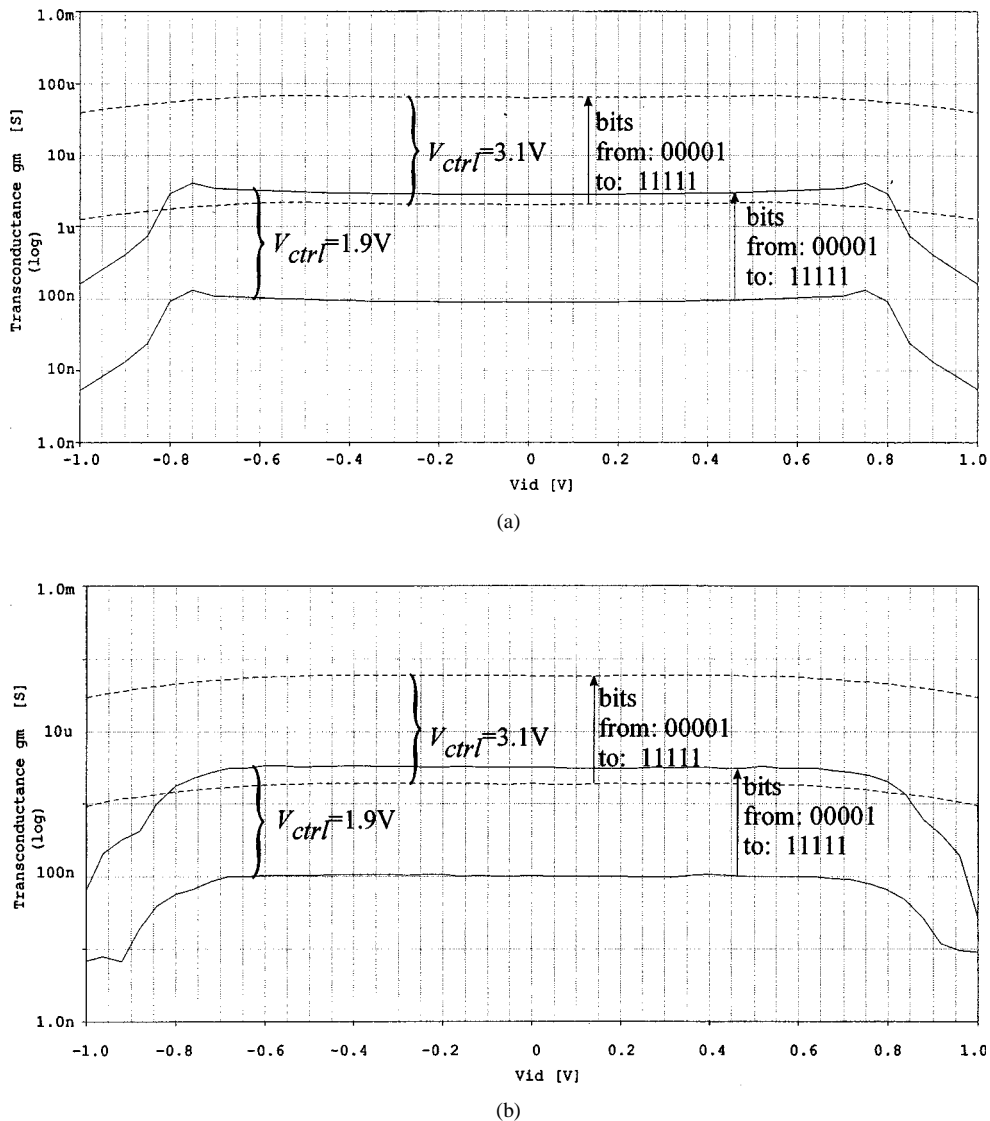
Fig. 5.   Simulated (a) and measured (b) transconductance of the programmable OTA in Fig. 4.

resistance. It was specified that the OTA should work linearly for input voltage range ± 0.5 V and when used in an integrator, it should have the dc gain greater than 40 dB. Due to the high output resistance, the dc gain obtained is well above 40 dB for all values of g_m in the operating range. The 3-dB frequency of the OTAs transfer function $I_{\text{out}}/V_{\text{id}}$ is over 20 MHz. The obtained maximum operation frequency f_{max} of the OTA, defined as the frequency at which the phase deviation from $-90°$ is $1°$ when the output is short-circuited, is about 3 MHz. This criterion is used for estimating the frequency range of the proper operation of filters.

Besides the digital programming of g_m using 5-bit control word, an additional transconductance change is obtained by means of analog voltage V_b. The transconductance of the OTA depends linearly on the voltage V_b as shown in (5). Voltage V_b can be set to any value in the range from about 22 mV up to about 500 mV which corresponds to the range of control voltage V_{ctrl} from 1.9 to 3.1 V. This makes g_m tunable by a factor of about 22.

D. Noise and Dynamic Range

Dynamic range (DR) of a circuit is normally defined as the ratio of the maximum and minimum signal levels, while the minimum and maximum signal levels are determined by the noise and distortion of the circuit, respectively [17]. To determine the DR of circuits such as filters, the following expression can be used [18]:

$$DR_{@n\%\text{THD}} = \frac{\frac{|\text{signal}|^2_{n\%\text{THD}}}{2}}{\overline{\text{noise}}^2} \qquad (6)$$

where $|\text{signal}|_{n\%\text{THD}}$ is the magnitude of the output signal when the filter circuit reaches $n\%$ of the total harmonic distortion (THD) and $\overline{\text{noise}}^2$ is the mean-squared value of the noise.

Another very useful measure called signal-to-noise ratio (SNR) is defined as the ratio of the mean-squared value of the signal to the mean-squared value of the noise. More detailed considerations of the SNR for the g_m-C filters can be found in the literature [19].

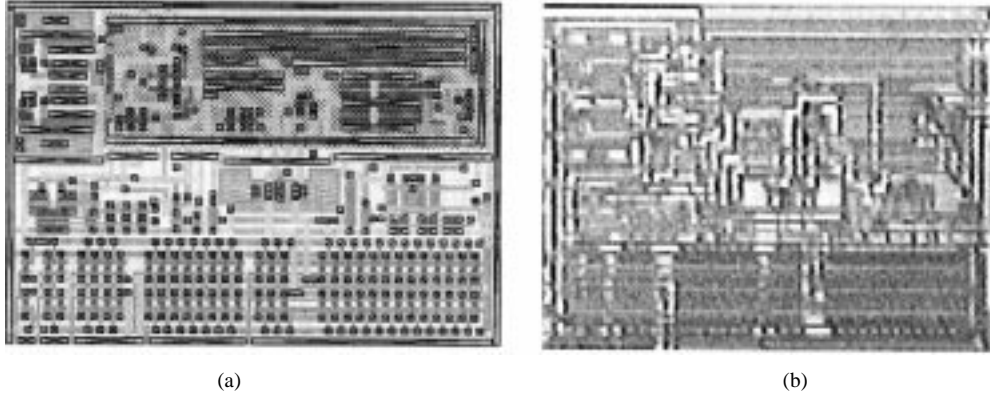(a)   (b)

Fig. 6.   Layout of the OTA in Fig. 4. (a) Design. (b) Photography.

A significant improvement in linearity and distortion reduction of the proposed OTA in Fig. 2 is obtained by cross-coupling differential MOS pairs. However, cross-coupling increases the noise of the OTA due to the effect of the g_m subtraction. For high-frequency operation of the OTA in Fig. 2, thermal channel noise is assumed to be the dominant noise source. Thus, the equivalent input-referred voltage noise can be approximated by [16], [20], [21] as

$$\frac{v_{ni}^2}{\Delta f} = \frac{16}{3}\frac{kT}{G_{m1}}(1+\chi)\left[\frac{2g_{m3,4}}{G_{m1}}\right] \tag{7}$$

where k is Boltzman's constant, T is the absolute temperature, $G_{m1} = g_{m1}-g_{m4} = g_{m2}-g_{m3}$, $g_{m1} = g_{m2}$, $g_{m3} = g_{m4} = g_{m3,4}$, and $\chi = g_{mb}/g_m$ with $g_{mb} = \partial i_D/\partial v_{BS}$. From (7), it is seen that optimum noise performance of the OTA stage is achieved by minimizing $g_{m3,4}$. However, this occurs at the expense of the decreased large signal capability and nonlinearity cancellation. There is tradeoff between noise performance and large-signal handling capability at the input of the cross-coupled OTA. Some simulation results confirming this were given in [16].

E. Second-Order Effects

Second-order effects such as mobility reduction, body effect and channel length modulation can cause deviations from ideal square-law behavior in MOS transistors and as a result, the transfer function given by (4) will no longer be strictly linear. The transconductance amplifier in Fig. 2 consists of two stages and each of them contributes its own part to the overall nonlinearity. Since current mirrors in the output stage cause errors in the output current about 10 times smaller than the input stage, considerations are, therefore, focused on the cross-coupled input cell.

An approximate analysis [16] which includes mobility reduction effect and body effect yields a condition under which transconductance stage $M1-M4$ remains linear, given by

$$\frac{K_{1,2}}{K_{3,4}} = \frac{[\theta(V_q + V_{T1,2}) - 1]^4}{[\theta(V_q + V_b + V_{T3,4}) - 1]^4} \tag{8}$$

TABLE I
SIMULATION RESULTS OF THE OTA IN FIG. 4

Parameter	Value
Maximal transconductance	63μS
Minimal transconductance	0.09μS
Resolution	5 bits
Ratio max./min. transconductance in the FPAA	31 times
Control range of the transconductance through voltage V_{ctrl}	>22 times

where $K_{1,2}$ and $K_{3,4}$ are transconductance parameters of transistors $M1$, $M2$ and $M3$, $M4$, respectively, $\theta = 1/(T_{OX}E_{CR})$ is the coefficient of the effect of the electric field on the mobility, (T_{OX} is the gate oxide thickness and E_{CR} is the critical field), $V_{Tn} = V_{To}+\gamma\left(\sqrt{\Phi - V_{BS}} - \sqrt{\Phi}\right)$, ($\Phi$ is the strong-inversion surface potential and γ is the bulk threshold parameter) and $V_q = (V_P + V_Q)/2$. Note, however, that scaling of W/L ratios of pairs $M1$, $M2$ and $M3$, $M4$ according to (1) and (2) is only possible for one given value of V_b.

The channel length modulation mainly causes the degradation in the output resistance of the MOS devices. But since in the output stage the cascoded mirror structure is used, the OTA output resistance remains high.

F. Simulation and Experimental Results

The OTA in Fig. 4 was simulated. Fig. 5(a) presents the simulated transconductance of the OTA for the minimum and maximum settings of the voltage V_b and the current gain A. The OTA in Fig. 4 was fabricated in ORBIT 2-μm CMOS technology. Its layout is shown in Fig. 6. Table I summarizes the achieved values of g_m. Experimental results from the fabricated chip are presented in Figs. 5(b) and 7.

IV. PROGRAMMABLE CAPACITOR ARRAY

The proposed structure of the programmable capacitor array is shown in Fig. 8. It consists of five capacitors C_0 to C_4 and switches S_{C_0} to S_{C_4}. The branch of capacitor C_0 and switch S_{C_0} represents the least significant bit (LSB). Each branch is built of an appropriate number of LSB branches (connected in parallel).
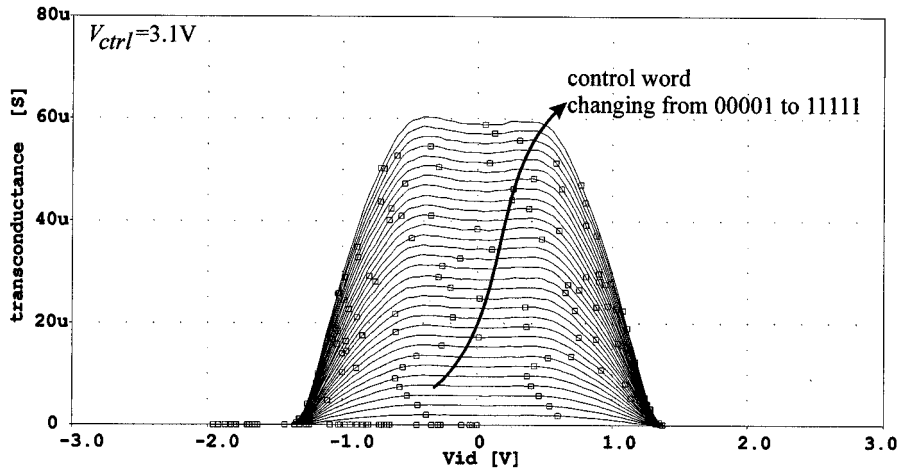
Fig. 7. Transconductance of the programmable OTA—experimental results for all values of control word and constant voltage $V_{\mathrm{ctrl}} = 3.1$ V.
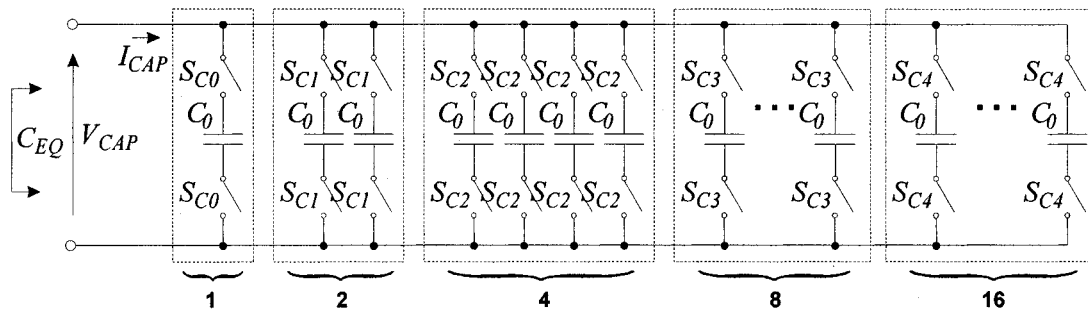

Fig. 8. Programmable capacitor array.

TABLE II
PARAMETERS OF PROGRAMMABLE CAPACITOR ARRAY IN FIG. 8

Parameter	Value
No of bits	5
Minimum capacitance $C_{EQ\min}$	1.5pF
Maximum capacitance $C_{EQ\max}$	15.5pF
Resolution ΔC_{EQ}	0.438pF
Current phase of the array for frequencies up to 10MHz	-90° ±1°
Occupied area of two capacitor arrays	360μm x 258μm

Switches are realized using MOSFETs of width high enough to achieve the current phase of a capacitor in the range of $-90°$ $\pm 1°$ for frequencies up to 10 MHz. The equivalent capacitance of the capacitor array can be expressed as

$$C_{EQ} = \sum_{n=0}^{4} b_n 2^n (C_{\mathrm{ON}} - C_{\mathrm{OFF}}) + C_{\mathrm{PAR}} \qquad (9)$$

where $b_n \in \{0, 1\}$, b_n is equal to 1 when switch S_{C_n} is ON and equal to 0 when S_{C_n} is OFF, C_{ON} and C_{OFF} are the capacitances of the LSB capacitor when switches S_{C_0} are in ON and OFF modes, respectively, while C_{PAR} is the parasitic capacitance of connections when all the switches are off. Table II summarizes the parameters of the programmable capacitor array.

V. TUNING OF g_m/C RATIO

This section is focused on the tuning technique used for measurements of the fabricated chip as well as on the proposed automatic tuning circuitry planned to be included in the next chip to be fabricated.

A. Tuning Using Four Lossy Integrators

The proposed FPAA includes three inputs and three outputs. This enables realization of up to three independent filters or other circuits working concurrently. Tuning of filters is based on small parameter differences between components inside the chip, so setting the reference integrator (or other reference circuit containing OTAs and Cs) to the desired g_m/C ratio will reflect on the filter characteristic frequency. Accuracy of such tuning is dependent on how precisely the desired g_m/C ratio can be achieved and the technology spread. Practical implementations provide 0.1%–5% accuracy [15], [22]–[25], [28].

Fig. 9 presents the block diagram of the tuning circuitry used during testing of the chip [15], [22]–[24], [28]. The upper part is the reference circuit consisting of 4 lossy integrators. The lower part is a tuned filter. All OTAs in the reference part as well as in the filter are identical and have the same value of control voltage V_{ctrl}. Comparison of integrator's phase delay with its desired value gives a signal which can be used in the manual or automatic correction of V_{ctrl}. Because the comparison of signals shifted by $-180°$ exactly is convenient, four integrators have
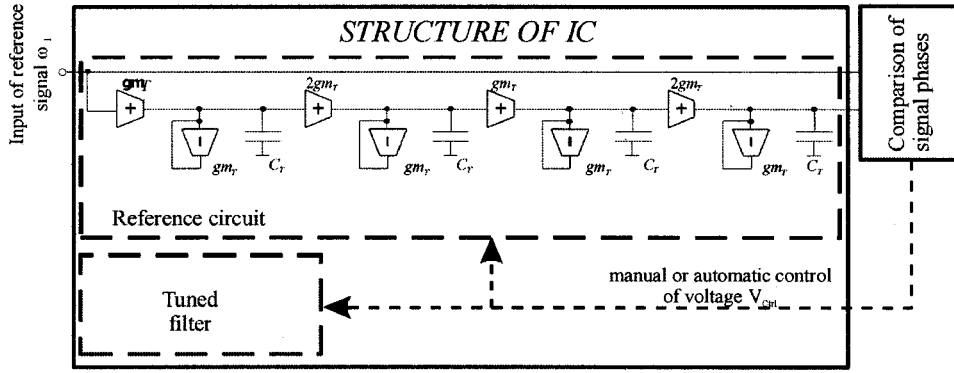
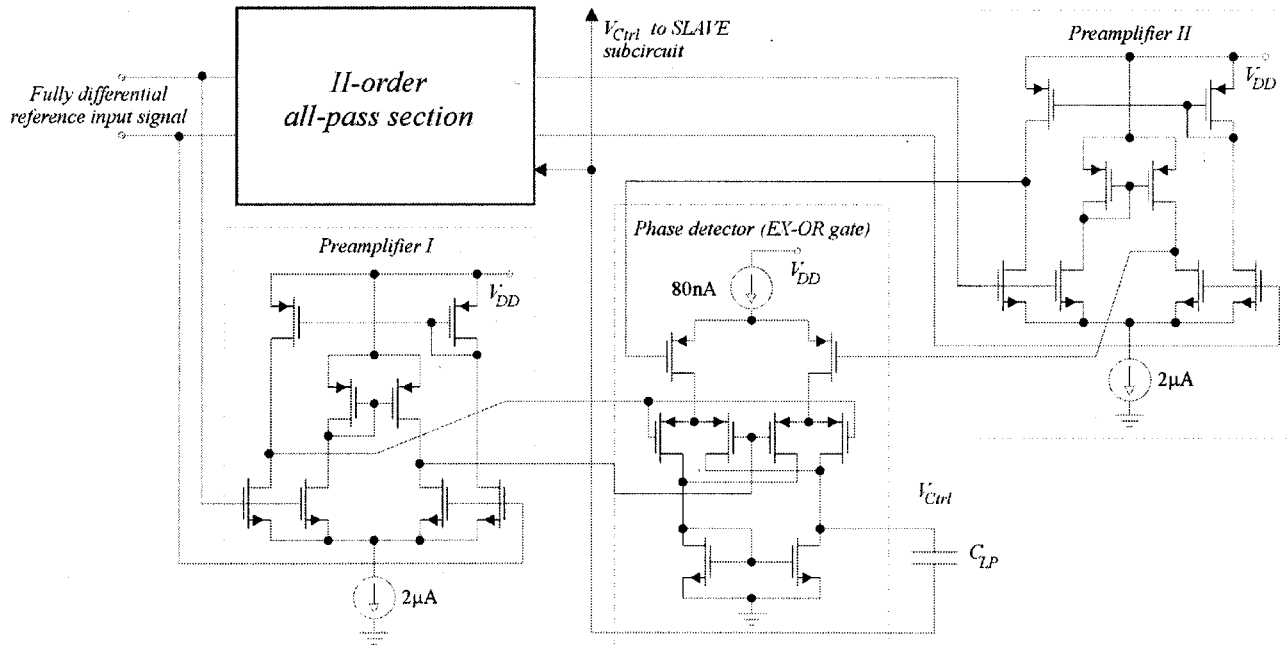Fig. 9.   Simplified schematic diagram of the proposed tuning circuit.

Fig. 10.   Simplified schematic of the proposed automatic tuning circuit (reference part).

been used, which give phase shift exactly equal to $-180°$ for frequency

$$\omega_I = \frac{gm_T}{C_T}. \qquad (10)$$

Assuming that time constant gm_i/C_j must be tuned to the frequency ω_Z, the frequency of the reference signal ω_I to be applied to the input of the reference path is:

$$\omega_I = \omega_Z \frac{gm_T}{gm_i} \frac{C_j}{C_T}. \qquad (11)$$

Having applied the reference signal, control voltage V_{ctrl} should be adjusted so that the phase shift of $-180°$ appears on the output of the reference path. Tuning accuracy depends on the precision of the phase detector (assuming equal delays on both paths). Using the oscilloscope, a $5°$ accuracy can be obtained. Because the reference path includes four integrators and the change in the frequency/phase characteristic for a lossy integrator at its unity frequency is $0.286\%/1°$, the overall precision can be established as $5°/4 \times 0.289\%/1° = 0.358\%$. In practice, tuning of the second-order bandpass filters realized

in our FPAA gives 2%–3% accuracy, depending on the chip unit and programmed filter frequency (not exceeding 300 kHz, because over this frequency parasitics of the switches significantly degrade the precision of the tuning). Thus the dominant factor is technology spread and better tuning can be achieved by redesigning OTAs and capacitors for better repeatability.

It is noted that, in Fig. 9, some of the OTAs in the reference path have actually a two-times greater transconductance. This provides the same amplitude of the compared signals.

B. On-Chip Automatic Tuning With Second-Order All-Pass Section

There are many automatic tuning circuits known in the literature. In most cases, they are quite complicated and often include phase-locked loops (PLLs), control loops [22]–[24] or use adaptive tuning [25]. In this paper a simple circuit is presented, which is planned to be included on the next chip to be fabricated. It consists (Fig. 10) of an all-pass second-order section (working as a reference circuit), EX-OR gate with two preamplifiers (working as a phase comparator) and single capacitor (working as the low-pass filter). The principle of operation is
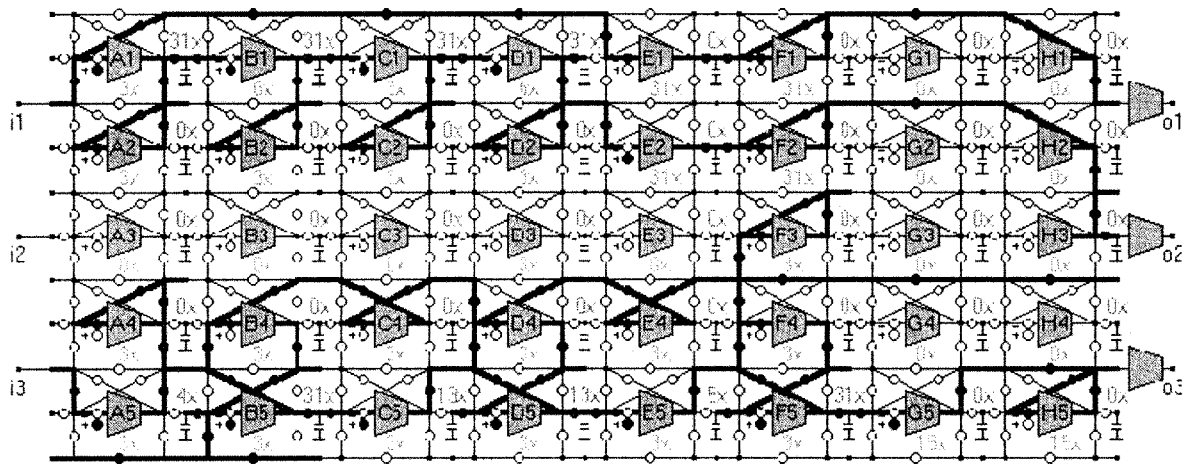
Fig. 11.   Structure of FPAA. Bold lines represent active connection, which realizes a sixth-order bandpass filter with tuning circuitry.

the same as the one in Fig. 9, with the difference that the desired phase shift of the all-pass section is $-90°$. The all-pass section gives comparable amplitudes of input and output signals with phases depending on the signal frequency and characteristic frequency of the section. For a second-order section there is only one point at which phase shift is equal to $90°$. Due to the constant amplitude of the all-pass section over a wide range of frequencies, the tuning circuit can be used in the wide spectrum of frequencies and always track the desired phase shift without multiple stable points. Of course, the errors caused by low loop gain, dc-offsets, mismatches at the phase detector's inputs and phase detector's error are high compared with the PLL method. However, design of the voltage-controlled oscillator (VCO) in the PLL circuit is more complicated than that of the all-pass section. In the presented circuit, errors of the phase comparator are dominant. Loop gain is very high because the capacitor is charged by a current source.

All subcircuits are biased with constant and relatively small currents (80 nA and 2 μA), which prevent cross-talk to a tuned slave circuit. Thus, the reference signal frequency can also be chosen in the passband of a tuned slave filter. Computer simulations using BSIM v3.2 models, show 1%–3% accuracy in the tuning of the characteristic frequency of the filter, depending on the conditions such as the desired frequency of the filter, filter configuration, temperature variations (in the range 0 °C–70 °C) and power supply voltage changes ($\pm 5\%$). Because of the low number of MOS transistors in series and switches being realized using the same devices, the circuit can function with low power supply voltage, starting from about 2.5 V (not taking into account the second-order all-pass section).

VI. FPAA USING CABs AND ITS APPLICATION IN OTA-C FILTER DESIGN

A. FPAA Using 40 CABs

The FPAA used for implementation of filters is presented in Fig. 11 (block diagram) and Fig. 12 (die photograph). It consists of 40 CABs from Fig. 1 positioned in eight columns and five rows. Additionally three OTAs $o1$–$o3$ act as signal buffers. Input signals are delivered through lines $i1$, $i2$ and $i3$. Because of this, up to three different filters can be realized simultaneously. The transconductance parameters of all the OTAs are controlled by
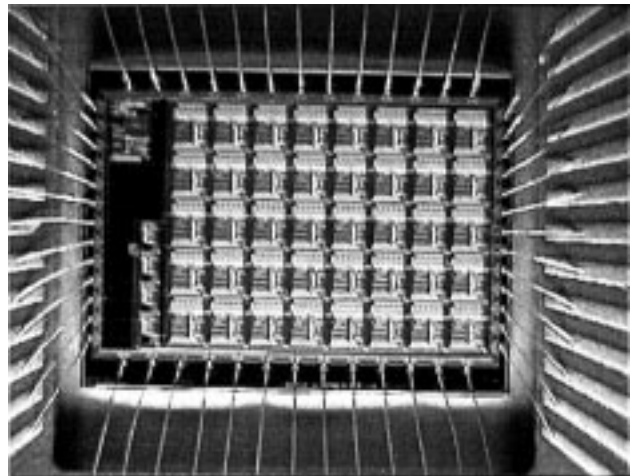

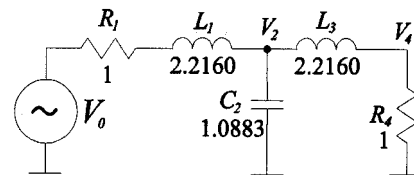Fig. 12.   Layout of matrix of 5 × 8 CABs in Fig. 11.

Fig. 13.   Third-order low-pass *RLC* prototype.

external voltage V_{ctrl} and through digital switching of the output current mirrors. While voltage V_{ctrl} is common for all the amplifiers in the array, it is still possible to set the transconductance of every OTA separately by setting the gain of the OTAs current mirror. Basic parameters of the OTA and programmable capacitor are presented in Tables I and II. The FPAA was physically implemented in the 2-μm n-well CMOS process through MOSIS. Programming of the FPAA is performed through serially shifting digital words of 880 bits.

B. Examples of Filter Design and Measurement Results

1) Implementation of Leapfrog OTA-C Filter Using FPAA: As the first example a sixth-order bandpass filter with center frequency $f_O = 60$ kHz and passband $BW = f_O$ is presented. The low-pass prototype (of third-order, 1-dB Chebyshev approximation [28]) is shown in Fig. 13. The filter
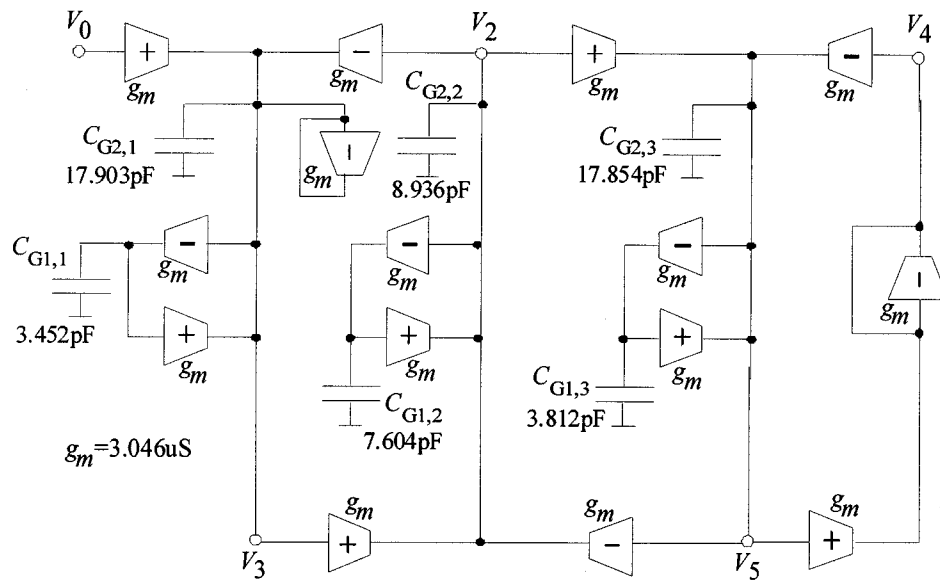
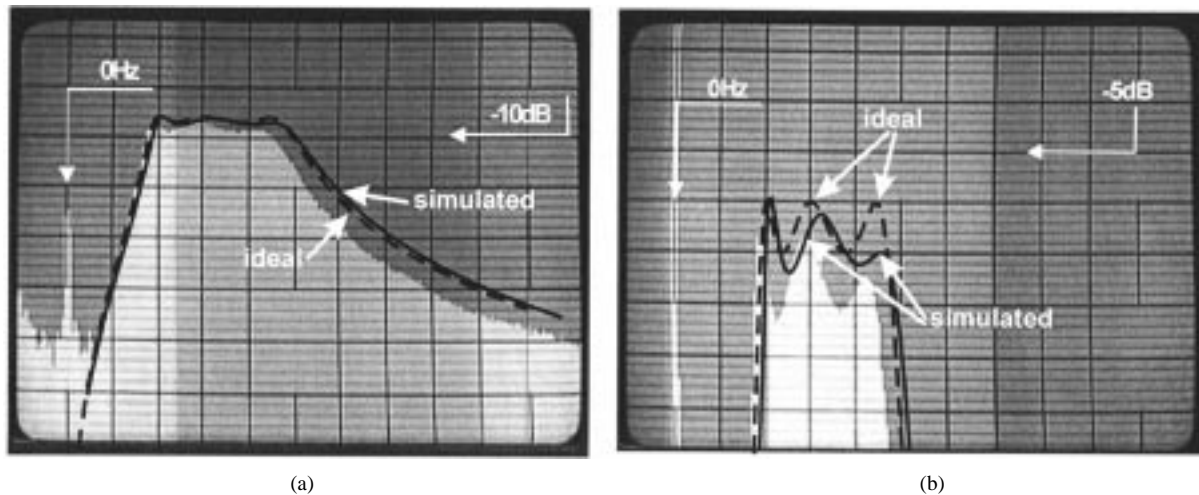Fig. 14.   OTA-C realization of the sixth-order bandpass filter.

Fig. 15.   Simulation and measurement results of sixth-order, 1-dB-ripple Chebyshev, bandpass filter. Center frequency is 60 kHz, passband 60 kHz. Screen photos with horizontal scale 20 kHz/div and (a) vertical scale 10 dB/div, (b) vertical scale 1 dB/div.

schematic diagram is presented in Fig. 14. Placement of Fig. 14 in the FPAA resources is shown in Fig. 11. The calculated values after low-pass to bandpass transformation have been rounded to the nearest value realizable in the FPAA. The capacitor's values also include the parasitic capacitances of switches and connections. Adjusting the analog voltage V_{ctrl} can change the center frequency of the filter about 22 times. In Fig. 11, the upper part (i.e., the first and the second row of CABs: A1-H1 and A2-H2) includes the tuning circuit described in Section V. Additionally, in the practically implemented tuning circuit in Fig. 11, OTAs $E1$ and $E2$ have opposite transconductance values, so the signals actually observed at the outputs $o1$ and $o2$ should have exactly the same phase (not $-180°$). Using (11), the frequency f_{i1} of the reference input signal can be calculated.

The filter was practically implemented in the structure of FPAA. Measurements were done using the Marconi TF 2370, Advantest TR4131E spectrum analyzer and Hewlett-Packard 3581A wave analyzer. The measured results are given in Fig. 15. Measurements have been taken after applying a signal

of frequency f_{i1} to the input $i1$ (Fig. 11) and manually setting the value of control voltage V_{ctrl} so that the signals observed at the outputs $o1$ and $o2$ were in exactly the same phase. This tuning technique was described in Section V-A. Comparing with the ideal characteristic, the filter exhibits no more than 1-dB error in the range 2–200 kHz. Switches placed in the paths conducting relatively large currents are the main cause of this error. The comparison of the simulated and measured noise, dynamic range and power dissipation is presented in Table III.

TABLE III
SIMULATION AND MEASUREMENT RESULTS OF THE SIXTH ORDER BANDPASS
FILTER WITH CENTER FREQUENCY $f_O = 60$ kHz AND PASSBAND $BW = f_O$

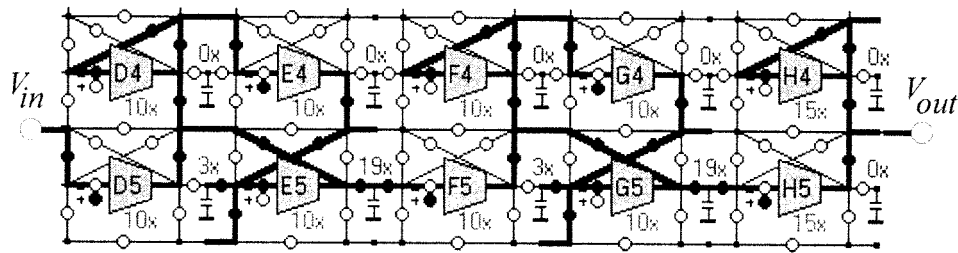| Parameter	Unit	Simulated	Measured
RMS input voltage $V_{in\ IP3}$ of signals causing IP3=-40dB, f_1=42.5kHz, f_2=45kHz	[mV]	90	156
RMS voltage V_{noise} of noise in 3dB passband of the filter referred to the input, f=39.3-99.65kHz	[mV]	0.438	0.622
Dynamic Range DR $(V_{in\ IP3} / V_{noise})$	[dB]	46.2	48
Power dissipation P_{tot}	[mW]	51.4	40.3

Fig. 16. Schematic diagram of the two biquad cascaded bandpass filter.

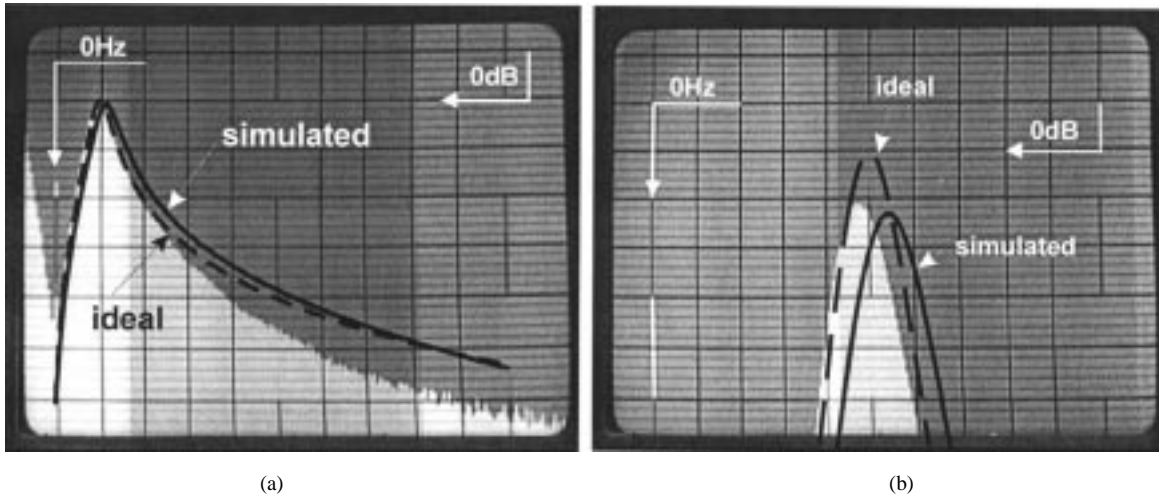(a)   (b)

Fig. 17. Simulations and measurement results of the two biquad cascaded bandpass filter. The center frequency is 500 kHz, and the quality factor of each section is $Q = 2$. Screen photos with (a) horizontal scale 500 kHz/div, vertical scale 10 dB/div, (b) horizontal scale 100 kHz/div, vertical scale 1 dB/div.

TABLE IV
SIMULATION AND MEASUREMENT RESULTS OF THE FOURTH-ORDER
BIQUAD CASCADED OTA-C FILTER WITH CENTER FREQUENCY
$f_O = 500$ kHz AND $Q = 2$

Parameter	Unit	Simulated	Measured
RMS input voltage $V_{in\ IP3}$ of signals causing IP3=-40dB, f_1=500kHz, f_2=550kHz	[mV]	120	21(*)
RMS voltage V_{noise} of noise in 3dB passband of the filter referred to the input, f=400-600kHz	[mV]	0.307	0.389(**)
Dynamic Range DR $(V_{in\ IP3} / V_{noise})$	[dB]	51.8	34.7
Power dissipation P_{tot}	[mW]	70.9	49.2

(*)significantly lower value than simulated, probably caused by OTAs input offsets voltages that narrow the linear range of OTAs dc characteristics.

(**) includes the noise of output buffers.

2) FPAA-Based Realization of Cascade OTA-C Filters: A fourth-order biquad cascaded OTA-C filter with center frequency $f_O = 500$ kHz and $Q = 2$ consisting of two biquad sections has been designed using the proposed FPAA, which is based on the structures well known in the literature [27], [28]. Design of the filter has been done taking into account the limitations of possible values of transconductances and capacitances (see Tables I and II). The tuning circuit described in Section V that enables to obtain an accurate g_m/C ratio has also been used. The filter was implemented in the FPAA (Fig. 16) and measurement results are given in Fig. 17 and Table IV.

VII. CONCLUSION

A high-frequency fully differential OTA with tunable and programmable transconductance has been analyzed, simulated, fabricated, and measured. A universal CAB consisting of the proposed OTA, programmable capacitor and switches has been developed. The CAB can be configured to perform the following functions: addition, subtraction, amplification, attenuation, integration and filtering of signals of frequencies from several kilohertz up to a few megahertz. The results of simulations and measurements confirm the possibility of realization of such functions. A test integrated circuit containing the array of 5×8 CABs has been fabricated in 2-μm CMOS technology and measured. The experimental results of the high-order bandpass OTA-C filters realized using the FPAA are close to the expected ones. Certain discrepancies are mainly caused by parasitic resistance and capacitance of switches. Due to the economical reasons, a cheap but somewhat out-of-date technology has been used for fabrication of the test chip. Realization of the proposed FPAA using modern submicron technology would result in a significant decrease of parasitic capacitances, thus providing a much higher operation frequency of the FPAA and its applications. Programmable analog circuits in comparison with custom designed circuits have a limited operating frequency due to the use of the switches. The future improved version of the circuit should contain an automatic offset compensation circuit for OTAs. The structure of the CAB

should also be changed in the way that the paths conducting large current would not contain switches.

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REFERENCES

[1] K. H. Loh, D. L. Hiser, W. J. Adams, and R. L. Geiger, "A robust digitally programmable and reconfigurable monolithic filter structure," in *Proc. IEEE Int. Symp. Circuits and Systems*, 1989, pp. 110–113.

[2] E. K. F. Lee and P. G. Gulak, "A CMOS field programmable analog array," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1860–1867, Dec. 1991.

[3] E. Pierzchala and M. A. Perkowski, "High-speed field programmable analog array architecture design," presented at the FPGA Symp., Berkeley, CA, Feb. 1994.

[4] E. Pierzchala, M. Perkowski, P. Van Halen, and R. Schaumann, "Current-mode amplifier/integrator for a field programmable analog array," in *IEEE Int. Solid State Circuits Conf. Tech. Dig.*, Feb. 1995, pp. 196–197.

[5] H. Kutuk and S. M. Kang, "A field-programmable analog array (FPAA) using switched-capacitor technique," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 4, May 1996, pp. 41–43.

[6] A. Bratt and I. Macbeth, "Design and implementation of a field programmable analogue array," in *Proc. FPGA*, 1996, pp. 88–93.

[7] S. H. K. Embabi, X. Quan, N. Oki, A. Manjrekar, and E. Sanchez-Sinencio, "A field programmable analog signal processing array," in *Proc. IEEE Midwest Symp. Circuits and Systems*, vol. 1, Aug. 1996, pp. 151–154.

[8] D. Anderson, C. Marcjan, D. Bersch, H. Anderson, P. Hu, O. Palusinski, D. Gettman, I. Macbeth, and A. Bratt, "A field programmable analog array and its application," in *IEEE Custom Integrated Circuits Conf.*, 1997, pp. 555–558.

[9] "MPAA020 Field Programmable Analog Array Datasheet," Motorola, 1997.

[10] X. Quan, S. H. K. Embabi, and E. Sanchez-Sinencio, "A current-mode based field programmable analog array architecture for signal processing applications," in *IEEE Custom Integrated Circuits Conf.*, 1998, pp. 277–280.

[11] V. C. Gaudet and P. G. Gulak, "CMOS implementation of a current conveyor-based field-programmable analog array," in *Asilomar Conf. Signals, Systems and Computers*, vol. 2, Nov. 1998, pp. 1156–1159.

[12] B. Pankiewicz, M. Wojcikowski, J. Jakusz, J. Glinianowicz, and S. Szczepanski, "A CMOS configurable analogue block for continuous-time programmable OTA-C filters," in *Proc. Eur. Conf. Circuit Theory and Design*, 1999, pp. 1019–1022.

[13] C. A. Looby and C. Lyden, "Op-amp based CMOS field-programmable analogue array," in *Proc. IEE Circuits Devices Systems*, vol. 147, Apr. 2000, pp. 93–99.

[14] R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," *IEEE Circuits Devices Mag.*, pp. 20–32, Mar. 1985.

[15] B. Nauta, *Analog CMOS Filters for Very High Frequencies*. Norwell, MA: Kluwer, 1993.

[16] S. Szczepanski, J. Jakusz, and R. Schaumann, "A linear fully balanced CMOS OTA for VHF filtering applications," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 174–187, Mar. 1997.

[17] G. Groenewold, "The design of high dynamic range continuous-time integratable bandpass filters," *IEEE Trans. Circuits Syst.*, vol. 38, pp. 838–852, Aug. 1991.

[18] J. Mahattanakul and C. Toumazou, "Current-mode versus voltage-mode $G_m - C$ biquad filters: What the theory says," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 173–186, Feb. 1998.

[19] G. Efthivoulidis, L. Tóth, and Y. Tsividis, "Noise in $G_m - C$ filters," *IEEE Trans. Circuits Syst.*, vol. 45, pp. 295–302, Mar. 1998.

[20] S. T. Dupuie and M. Ismail, "High frequency CMOS transconductors," in *Analogue IC Design: The Current-Mode Approach*, C. Toumazou, F. J. Lidgey, and D. G. Haigh, Eds. Stevenage, U.K.: Peregrinus, 1990.

[21] G. Niccollini, D. Pancini, and S. Pernici, "Simulation-oriented noise model for MOS devices," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1209–1212, Dec. 1987.

[22] J. M. Khoury, "Design of a 15 MHz CMOS continuous-time filter with on-chip tuning," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1988–1997, Dec. 1991.

[23] F. Krummenacher and N. Joehl, "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 23, pp. 750–757, June 1988.

[24] M. Banu and Y. Tsividis, "An elliptic continuous-time CMOS filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 1114–1121, Dec. 1985.

[25] K. A. Kozma, D. A. Johns, and A. S. Sedra, "Automatic tuning of continuous-time integrated filters using an adaptive filter technique," *IEEE Trans. Circuits Syst.*, vol. 38, pp. 1241–1248, Nov. 1991.

[26] G. Di Cataldo, G. Palumbo, and S. Stivala, "New CMOS current mirrors with improved high-frequency response," *Int. J. Circuit Theory and Applications*, vol. 21, pp. 443–450, 1993.

[27] T. Deliyannis, Y. Sun, and J. K. Fidler, *Continuous-Time Active Filter Design*. Boca Raton, FL: CRC, 1999.

[28] R. Schaumann, M. S. Ghausi, and K. R. Laker, *Design of Analog Filters: Passive, Active RC and Switched Capacitor*. Englewood Cliffs, NJ: Prentice-Hall, 1990.

[29] M. E. Valkenburg, *Analog Filter Design*. New York: CBS College Publishing, 1982.

[30] "New Dimensions in ISP Programmable Analog Circuit," Lattice Semiconductor Corp., Hillsboro, OR, 1999.

[31] The AN10E40 Field Programmable Analog Array. Anadigm Co, Crewe, U.K. [Online]. Available: http://www.anadigm.com

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