A robust high-efficiency cross-coupled charge pump circuit without blocking transistors

***Abstract*—A fully integrated cross-coupled charge pump circuit with a new clock scheme has been presented in this paper. The new clock scheme ensures that all NMOS pre-charge transistors are turned off when the voltages of main clock signals are high. Notably, all PMOS transfer transistors will be turned off when the voltages of the main clock signals are low. As a result, the charge pump eliminates all of the reversion power loss and reduces the ripple voltage. The proposed charge pump has a better performance even in scenarios where the main clock signals are mismatched. The proposed charge pump circuit was simulated using Spectre in the TSMC 0.18 μm CMOS process. The simulation results show that the proposed charge pump circuit has a high voltage conversion efficiency and low ripple voltage.**

***Index Terms*— Cross-coupled charge pump; Reversion power loss; Ripple voltage**

I. Introduction

CHARGE pump circuits have been often used to convert a DC input voltage to a DC output voltage, they can generate a voltage larger than the supply voltage or lower than the ground of the chip. Consequently, charge pumps can provide tens or hundreds of mA current for subsequent signal processing blocks. However, to supply a stable and higher DC voltage to all the embedded Intellectual Properties (IPs) has become an important challenge. The advantages of charge pump circuits are low cost, low EMI (Electro-Magnetic Interference), and small size. For these reasons, the design issues are always focused on high pump-efficiency, high power-efficiency, higher output power, and low output ripple voltage.

In 1976, J. F. Dickson proposed a Dickson charge pump with diode-connected NMOS transistors instead of diodes. This kind of charge pump can be easily implemented in a standard CMOS process [1]. However, due to the body effect, the high NMOS transistor threshold voltage reduces the boost efficiency. Accordingly, J. T. Wu and K. L. Chang proposed dynamic charge transfer switches (CTS) instead of diode-connected NMOS transistors, making sure the NMOS transistors are fully opened to eliminate the threshold voltage [2]. However, in multi-stage charge pump circuits, diode-connected CMOS transistors still exist in the final output stage. This leads to a certain threshold loss problem, while the substrate effect still exists. Cross-coupled voltage doublers are widely used, due to its less voltage drop between the drain terminal and the source terminal of each switch. The main disadvantage of Cross-coupled voltage doublers is that they have three kinds of reversion loss: the reversion loss from the output to the flying capacitors, the reversion loss from the flying capacitors to the input, and the reversion loss from the output to the input [3]. Many other technologies, like the Break-Before-Make mechanism, the first-level gate-control mechanism, new gate control strategies, transfer blocking technique and modified pre-charge scheme, are proposed to eliminate the reversion loss in the conventional cross-coupled voltage doublers [4-10]. However, some of these technologies need extra level shifters or blocking transistors, some of them have lower pumping efficiency or higher power consumption, most of them do not analyze the situation with mismatched main clock signals.

In this work, a new gate cross-coupled charge pump circuit with a new clock scheme has been proposed to eliminate the reverse current and improve the voltage conversion efficiency. After an overview of conventional CMOS charge pumps in Section II, the proposed charge pump is described in Section III. Section IV presents comparison and discussion to evaluate the performance of the proposed charge pump. Conclusions are presented in Section V.

II. Solution of Traditional Charge Pump

In [1], dealing with research theme of charge pump circuits, the Dickson charge pump is shown in Fig.1. It is based on a MOS diode connection chain. In this charge pump, flying capacitors are switched by double non-overlapping clocks and the output voltage, pumped stage by stage, is higher than the input DC voltage. However, the threshold-drop exists in each diode-connected CMOS transistor. This is a serious problem for voltage conversion in every stage. The output voltage of the Dickson charge pump can be expressed as:

$$V_{out} = V_{in} + N\left[\left(\frac{C}{C+Cs}\right)V_{in} - V_{th} - \frac{I_{out}}{f(C+Cs)}\right] - V_{th} \qquad (1)$$

Where V_{th} is the supply voltage of systems, V_{out} is the output voltage which is pumped from the input voltage. V_{th} is the threshold voltage of NMOS transistors, *C* is the flying capacitor, C_s is the stray capacitance, and N is the number of stages. From this equation, we know the threshold-drop will exist at every stage, even in the output stage, this problem will reduce the pump-efficiency seriously.

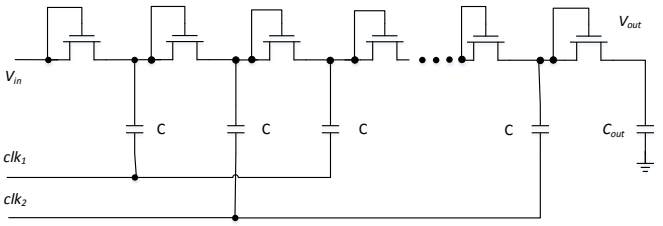

Fig. 1. Schematic of Dickson charge pump.

To solve the threshold loss problem of the Dickson charge pump, cross-coupled charge pumps have been proposed to reduce the output voltage ripple. However, the presence of reverse charge seriously affects the efficiency of voltage conversion.

Traditional cross-coupled charge pump circuit is shown in Fig.2 (a). It consists of a pre-charge circuit with a pair of cross-

coupled NMOS pre-charge transistors (M_{n1} and M_{n2}), two flying capacitors (C_1 and C_2), and two serial cross-coupled PMOS transfer transistors (M_{p1} and M_{p2}) acting as charge-transfer devices to generate a higher output voltage (V_{out}).

During the clock transitions shown in Fig.2 (b), when the voltage of clk_1 goes low, and the voltage of clk_2 is not high enough to turn off the transfer transistor (M_{p1}), there will be a reverse current called output loss. Similarly, when the voltage of clk_2 goes low, and the voltage of clk_1 is not high enough to turn off the transfer transistor (M_{p2}), there will also be a reverse current called output loss. The output loss is a current from the output node to the flying capacitors.

When the voltage of clk_1 goes high, and the voltage of clk_2 is not low enough to turn off the pre-charge transistor (M_{n1}), there will be a reverse current called pumping loss. Similarly, when the voltage of clk_2 goes high, and the voltage of clk_1 is not low enough to turn off the pre-charge transistor (M_{n2}), there will also be a reverse current called pumping loss. The pumping loss is a current from the flying capacitors to the input node.

When the transistors M_{p1}, and M_{n1} or M_{p2}, and M_{n2} are turned on at the same time, there will be a reverse current called short-circuit loss. The short-circuit loss is a current from the output node to the input node.

This means that the cross-coupled charge pump can solve the threshold voltage problem in [3]. However, the disadvantage of reversion current seriously reduces the voltage conversion efficiency.

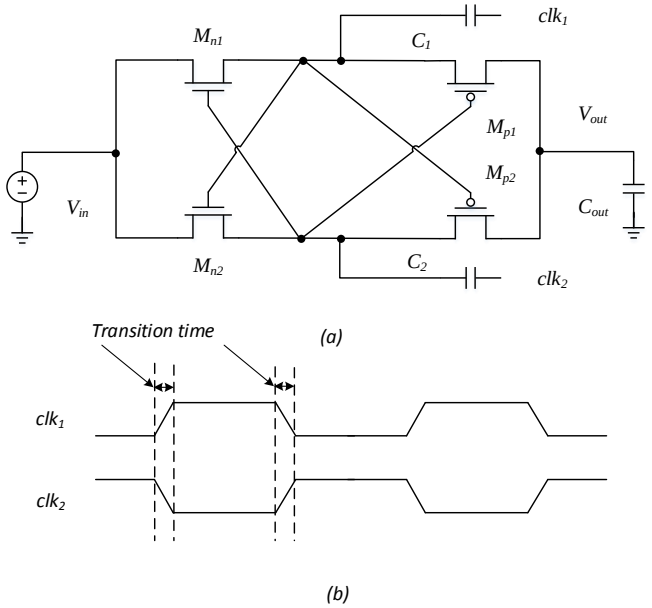

Fig. 2. (a) Conventional cross-coupled charge pump. (b) The overlapped intervals existing at clock transitions.

These reversion charges can be reduced or eliminated using several techniques [4-10], however, only transfer blocking technique works when the main clock signals are mismatched, and a further improvement can be made to increase the transfer efficiency of those circuits with transfer blocking technique. In this paper, an improved cross-coupled charge pump and its control scheme are proposed to increase the transfer efficiency without reversion current.

The charge pump with transfer blocking transistors is shown in Fig. 3. The main components are in the dotted box. It contains a pre-charge circuit with a pair of cross-coupled NMOS pre-charge transistors (M_{n1} and M_{n2}), two flying capacitors (C_1 and C_2) and two serial cross-coupled PMOS transfer transistors (M_{p1} and M_{p2}) acting as charge-transfer devices to generate a higher output voltage (V_{out}).

Compared to the conventional cross-coupled charge pump, two switches and a *TCO* signal (a local boosted control signal) have been added to block the reverse current from the output node to the flying capacitors. The *TCO* is enabled before the start of main clock transition time and disabled after the end of the transition time. Therefore, we can make sure that the voltage of *TCO* is high enough to turn off the switches from the start to the end of main clock transitions. This means no output loss exists.

The auxiliary NMOS transistors (M_{sn1}, M_{sn2}), capacitors (C_{sn1}, C_{sn2}) and a control signal generator have been added to generate a control signal to eliminate the reverse current from the flying capacitors to the input node. The voltage of the generated control signal for NMOS pre-charge transistor M_{n1} is low when the voltage of leading clk_1 or lagging clk_1 is high. Therefore, we can make sure the gate voltage of M_{n1} is low enough to turn off M_{n1} from the rising edge to the falling edge of clk_1. Similarly, the voltage of the generated control signal for NMOS pre-charge transistor M_{n2} is low when the voltage of leading clk_2 or lagging clk_2 is high. Therefore, we can make sure the gate voltage of M_{n2} is low enough to turn off M_{n2} from the rising edge to the falling edge of clk_2. This means no pumping loss exists. The short-circuit loss also does not occur since transistor pair $\frac{M_{n1}}{M_{p1}}$ or $\frac{M_{n2}}{M_{p2}}$ cannot be turned on simultaneously.

Actually, the switches ($S_{1,2}$) in this circuit are two PMOS transistors. Obviously, the conduction loss, caused by non-zero ON resistance of switches as a result of the voltage drop across the drain-source terminals of transistors, will decrease the transfer efficiency.

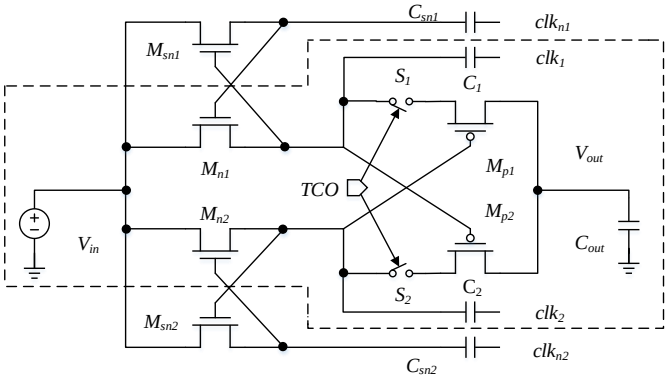

Fig. 3. Charge pump with transfer blocking transistors.

III. Proposed Charge Pump Circuit

The proposed charge pump has been shown in Fig. 4. Compared with the charge pump with transfer blocking transistors, we eliminate those switches and add auxiliary transistors (M_{sp1},M_{sp2}) and capacitors (C_{sp1},C_{sp2}).

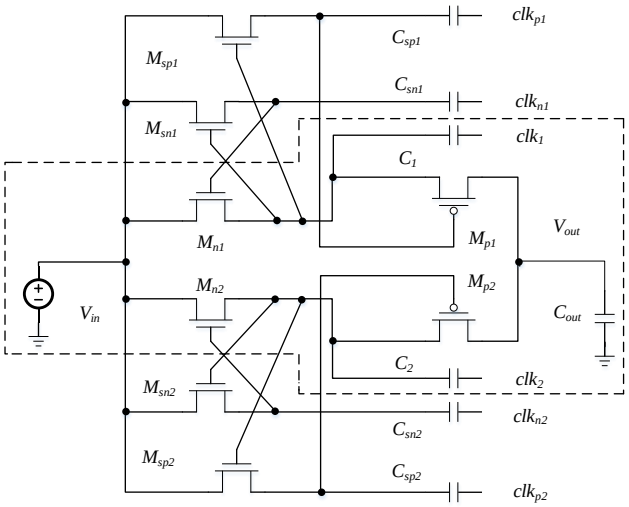

Fig. 4. The proposed charge pump.

All clock signals are generated from a pair of differential input clock signals (clk_{in1} and clk_{in2}). The structure of the control signal generator for the proposed charge pump is shown in Fig. 5. Main clocks ($clk_{1,2}$) are the buffered version of input clocks (clk_{in1} and clk_{in2}). Other signals are generated by monitoring the relative timing of rising and falling edges of input clocks and the buffered version of input clocks.

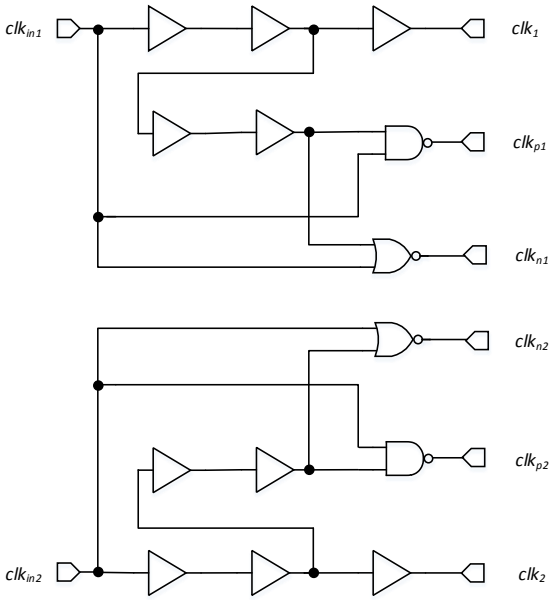

Fig. 5. Control circuits.

The relationship between $clk_{n1,2}$ and $clk_{1,2}$ is shown in Fig. 6 (a). From Fig. 6 (a), we can see that the voltage of clk_{n1} will be low when the voltage of clk_{in1} or lagging clk_1 is high, and the voltage of clk_{n2} will be low when the voltage of clk_{in_2} or lagging clk_2 is high. Therefore, during the transition time, the voltage of clk_{n1} or clk_{n2} will be low to make sure main NMOS transistors (M_{n1} or M_{n2}), in the dotted box of Fig. 4, will be turned off. This means the pumping loss will be eliminated.

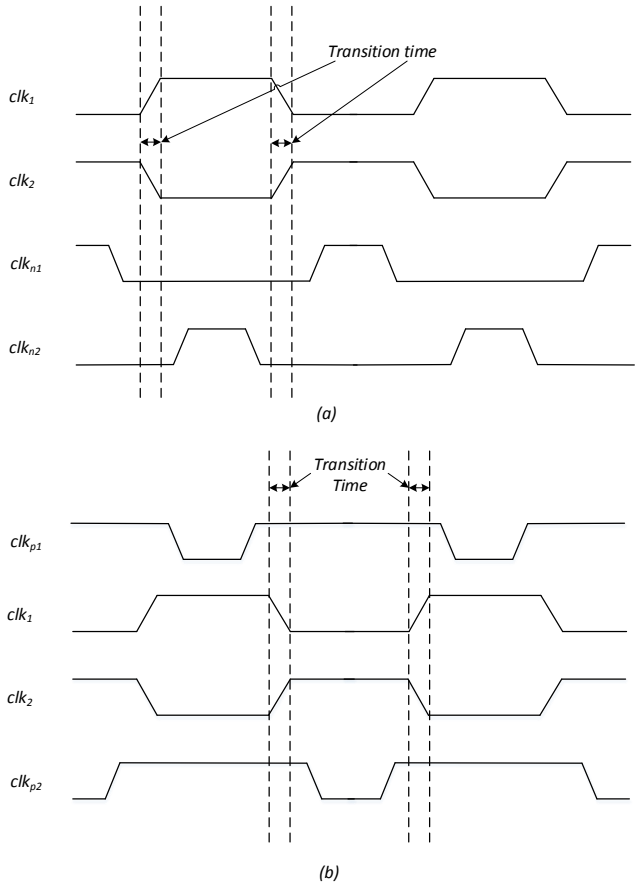

Fig. 6. The matched situation (a) The relationship between $clk_{n1,2}$ and $clk_{1,2}$. (b) The relationship between $clk_{p1,2}$ and $clk_{1,2}$.

The relationship between $clk_{p_{1,2}}$ and $clk_{1,2}$ is shown in Fig. 6(b). From Fig. 6 (b), we can see that clk_{p1} will be high when the voltage of clk_{in1} or lagging clk_1 is low, and clk_{p2}will be high when the voltage of clk_{in2} or lagging clk_2 is low. Therefore, during the transition time, clk_{p_1} or clk_{p2} will be high to make sure main PMOS transistors (M_{p1} or M_{p2}), in the dotted box of Fig. 4, will be turned off. This means the output loss will be eliminated.

When the main clock signals are mismatched, the relationship between all clock signals has been shown in Fig. 7. We will see that we can still eliminate all reversion current regardless of the mismatched main clock signals.

From Fig. 7 (a), we can see that the voltage of $clk_{n1,2}$ is low to turn off the NMOS transistors, when the voltage of $clk_{1,2}$ is high in the time duration of $t_{1,2}$ so the pumping loss is eliminated. Similarly, from Fig. 7 (b), we can see that, in the time duration of $t_{3,4}$, the voltage of $clk_{1,2}$ is low and the voltage of $clk_{p1,2}$ is high to turn off the PMOS transistors. Therefore the output loss is eliminated.

NMOS transistors are turned on only when the voltage of clk_1 is low and the voltage of clk_{n1} is high. PMOS transistors are turned on only when the voltage of clk_1 is high and the voltage of clk_{p1} is low. Therefore, NMOS transistors and PMOS transistors will never be turned on at the same time to make sure the short circuit loss has been eliminated.

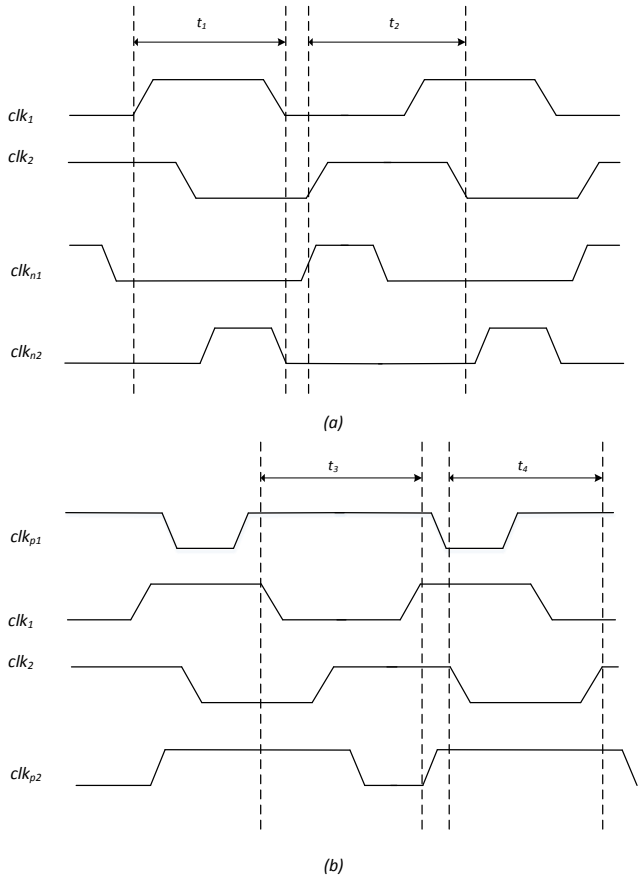

Fig. 7. The mismatched situation (a) The relationship between $clk_{n1,2}$ and $clk_{1,2}$. (b) The relationship between $clk_{p1,2}$ and $clk_{1,2}$.

The single-stage charge pump can be cascaded to obtain a higher output voltage. As a result, a single-stage charge pump without load can provide an output voltage of $2\,V_{in}$. Multiple single-stage cross-coupled circuits can be cascaded to obtain a high output voltage, ideally, an n-stage gate-cross-coupled circuit can get an output voltage of $(n\ +\ 1)V_{in}$.

In [3], a multi-stage gate-coupled charge pump circuit is proposed. Considering the reversion loss and the substrate effect, the output voltage is lower than the ideal voltage, and the power conversion efficiency is very low. With the increase of the stage, the source voltage of NMOS transistors is increasing and the substrate effect seriously affects the efficiency of the charge pump.

In this work, all bodies of NMOS transistors have been connected to the input point and all bodies of PMOS transistors have been connected to the output point to eliminate potential substrate effects. The proposed n-stage charge pump, based on n proposed single-stage charge pumps, is shown in Fig. 8.

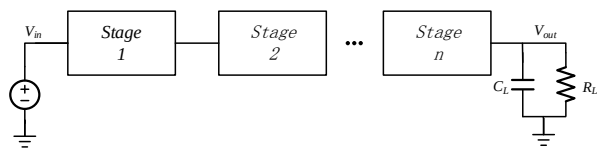

Fig. 8. Illustration of the proposed n-stage charge pump.

IV. Simulation Results

The proposed charge pump was simulated in 0.18μm CMOS technology. In the proposed design, both of the flying capacitors and the output capacitor are 30 pF. The auxiliary capacitors are 2 pF. Simulation results of the circuit were compared. In order to ensure a fair comparison of the proposed design to other designs, all of the flying capacitors, output capacitors and the transferring switches in these designs are chosen with the same specifications. Fig. 9 shows us the voltage conversion ratio versus supply voltage. The simulated voltage conversion ratio of the charge pumps in [8] is 1.96–1.98 and proposed charge pump reaches around 1.964–1.992. These results show that the proposed charge pump provides up to 0.6% improvement over the charge pump in [8].

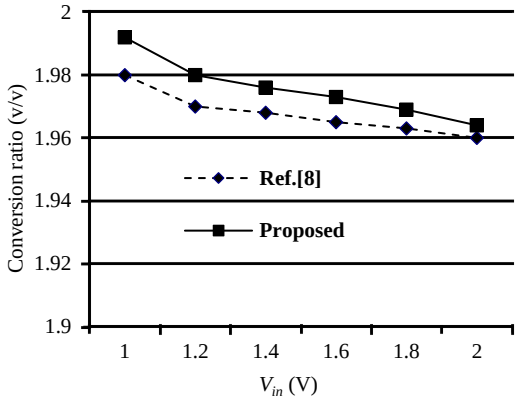

Fig. 9. Voltage conversion ratio versus supply voltage.

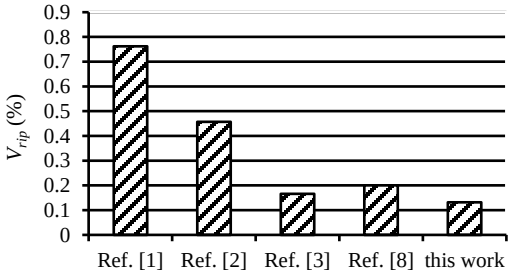

Fig. 10. Output ripple voltage comparison.

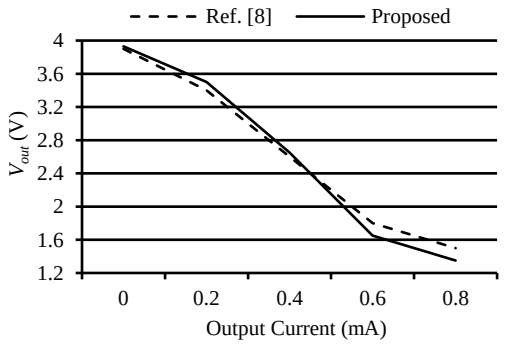

Fig. 11. Output voltage versus output current.

In Fig. 10, the new charge pump is compared with the circuits

in [1-3] and [8] with a load current of 20 μA. The ripple voltage of the new charge pump is significantly smaller than that of the conventional cross-coupled charge.

To evaluate the performance in terms of driving capability, output voltages of charge pumps with various loading currents at 2 V supply are compared in Fig. 11. For the loading current of 0–0.8 mA, the output voltage of the proposed charge pump drops from 3.93 to 1.35 V, which is almost as good as the charge pump in [8].

V. Conclusions

This paper has presented a new charge pump circuit with a new control method. The proposed structure eliminates all reversion power losses without blocking transistors. The simulation results show that we can get a robust higher output voltage and a low ripple voltage compared with some published results. What's more, this design does not require any extra level shifter circuit and both of gate-to-source/drain voltages and drain-to-source voltages do not exceed the nominal supply.

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A robust high-efficiency cross-coupled charge pump circuit without blocking transistors

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***Abstract*—A fully integrated cross-coupled charge pump circuit with a new clock scheme has been presented in this paper. The new clock scheme ensures that all NMOS pre-charge transistors are turned off when the voltages of main clock signals are high. Notably, all PMOS transfer transistors will be turned off when the voltages of the main clock signals are low. As a result, the charge pump eliminates all of the reversion power loss and reduces the ripple voltage. The proposed charge pump has a better performance even in scenarios where the main clock signals are mismatched. The proposed charge pump circuit was simulated using Spectre in the TSMC 0.18 μm CMOS process. The simulation results show that the proposed charge pump circuit has a high voltage conversion efficiency and low ripple voltage.**

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