Design of High Efficiency Cross-Coupled Charge Pump Circuit with Four-clock Signals

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Abstract—**A fully integrated cross-coupled charge pump circuit for boosting dc-to-dc converter applications with four-clock signals has been proposed. With the new clock scheme, this charge pump eliminates all of the reversion power loss and reduces the ripple voltage. In addition, the largest voltage differences between the terminals of all transistors do not exceed the power supply voltage to solve the gate-oxide overstress problem in the conventional charge pump circuits and enhance the reliability. This proposed charge pump circuit does not require any extra level shifter, therefore the power efficiency is increased. The proposed charge pump circuit has been simulated using Spectre in the TSMC 0.18μm CMOS process. The simulation results show that the maximum voltage conversion efficiency of the new 3-stage cross-coupled circuit with an input voltage of 1.5V is 99.8%. According to the comparison result of the conventional and this enhanced charge pump, the output ripple voltage has been significantly reduced.**

Keywords—Cross-coupled charge pump; Reversion power loss; Ripple voltage; Four-clock signal

I. INTRODUCTION

Using switched-capacitor charges, charge pump circuits have been often used to convert a dc input voltage to another dc output voltage, it can generate a voltage larger than the supply voltage or lower than the ground of the chip. Charge pumps can provide tens or hundreds of mA current for subsequent signal processing blocks. Supplying a stable and higher DC voltage to all the embedded Intellectual Properties (IPs) becomes an important challenge. The advantage of charge pump circuits is low cost, low EMI and small size. For these reasons, the design issues are always focused on high pump-efficiency, high power-efficiency, higher output power, and low output ripple voltage.

In 1976, J. F. Dickson proposed a Dickson charge pump with diode-connected NMOS transistors instead of diodes. This kind of charge pump can be easily implemented in a standard CMOS process [1]. However, due to the body effect, the high NMOS transistor threshold voltage reduces the boost efficiency. J. T Wu and K. L Chang proposed dynamic charge transfer switches (CTS) instead of diode-connected NMOS transistors, making the NMOS fully open to eliminate the threshold voltage [2]. However, in multi-stage charge pump circuits, diode-connected CMOS transistors still exist in the final output stage. This will lead to a certain threshold loss problem, while the substrate effect still exists. Cross-coupled voltage doublers are widely used, due to its less voltage drop between the drain terminal and source terminal of each switch. The main disadvantage of Cross-coupled voltage doublers is that they have three kinds of reversion loss: the reversion loss from the output to the

flying capacitors, the reversion loss from the flying capacitors to the input, the reversion loss from the output to the input [3]. The break-before-make mechanism, the first-level gate-control mechanism, new gate control strategies, transfer blocking technique and modified pre-charge scheme are proposed to eliminate the reversion loss in the conventional cross-coupled voltage doubler, however, we need extra level shifters or blocking transistors, all these will degrade the pumping efficiency, the stability or increase the power consumption [4-7].

In this work, a new gate cross-coupled charge pump circuit has been proposed to eliminate the reverse current and a special bias method has also been proposed to reduce the substrate effect and improve the voltage conversion efficiency.

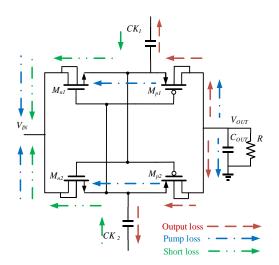## II. SOLUTION OF TRADITIONAL CHARGE PUMP

In [1], dealing with research theme of charge pump circuits, the Dickson charge pump is proposed. It is based on a CMOS diode connection chain. In this charge pump, pump Capacitors are switched by double non-overlapping clocks and the output voltage, pumped stage by stage, is higher than the input DC voltage. However, the threshold-drop exists in each diode-connected CMOS transistor, it's a serious problem for voltage conversion in every stage. The output voltage of the Dickson charge pump can be expressed as:

$$V_{OUT} = V_{IN} + N\left[\left(\frac{C}{C+C_s}\right)V_{IN} - V_{th} - \frac{I_{out}}{f(C+C_s)}\right] - V_{th} \qquad (1)$$

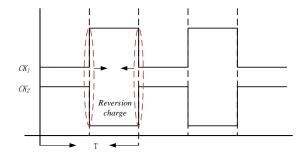Where V_{IN} is the supply voltage of systems, V_{OUT} is the output voltage which is pumped from the input voltage. V_{th} is the threshold voltage of NMOS transistors, C is the pump-capacitor, C_s is the stray capacitance, and N is the number of stages. From this equation, we can know the threshold-drop will exist at every stage, even in the output stage, this problem will reduce the pump-efficiency seriously.

To solve the threshold voltage problem of the Dickson charge pump, cross-coupled

charge pumps have been proposed to reduce the output voltage ripple. However, the presence of reverse charge seriously affected the efficiency of voltage conversion.

Traditional cross-coupled charge pump circuit is shown in Fig. 1 (a). During the clock transitions shown in Fig. 1 (b), when the voltage of CK_1 or CK_2 goes low, and the transistor M_{p1} or M_{p2} is still turned on, there will be a reverse current labeled as output loss. It is a current from the output node to the pump capacitor. Similarly, when the voltage of CK_1 or CK_2 goes high, and the transistor M_{n1} or M_{n2} is still turned on, there will be a reverse current labeled as pump loss. It is a current from the pump capacitor to the input node. When the transistors M_{p1}, and M_{n1} or M_{p2}, and M_{n2} are turned on at the same time, there will be a reverse current labeled as Short-circuit loss. It is a current from the output node to the input node. This means the cross-coupled charge pump can solve the threshold voltage problem [3]. However, the disadvantage of reversion charges seriously reduces the voltage conversion efficiency. In this paper, an improved cross coupled charge pump and its control scheme are proposed to eliminate the reversion power losses. Furthermore, the gate-to-source and source-to-drain voltages of each transistor are limited within the supply voltage (VDD). As a result, such a design can be easily scaled to multiple stages without encountering voltage overstress issues.

(a) Conventional cross-coupled voltage doubler and reversion loss paths

(b) The overlapped intervals existing at clock transitions

Fig. 1. Conventional cross-coupled charge pump

III. PROPOSED CHARGE PUMP CIRCUIT

In order to improve the efficiency of the traditional charge pump, all of the reversion loss paths, shown in Fig. 1, must be removed. For instance, to remove the power loss from the output to the flying capacitor, M_{p1} must be turned off before CK_1 goes low. Similarly, M_{n1} must be turned off before CK_1 goes high to remove the pump loss from the flying capacitor to the power supply. To remove the short- circuit loss from the output node to the power supply, M_{p1} and M_{n1} cannot conduct at the same time during the clock transition. Since the structure of traditional charge pump is symmetric, the other three loss paths can be removed in the same way. Meanwhile, eliminating the substrate effect, all bodies of PMOS transistors are connected to the output voltage of the present stage and all bodies of NMOS transistors are connected to the input voltage of the present stage. Therefore, we can make sure all bodies of PMOS transistors are connected to high voltage, and all bodies of NMOS transistors are connected to low voltage. By these means, all leakage currents have been reduced and the power supply efficiency has been optimized.

The two charge-transfer transistors, M_{n1} and M_{p1}, must be driven separately to make sure they will not conduct at the clock transition to eliminate the short-circuit loss. The gate-drive signals of $M_{n1,2}$ and $M_{p1,2}$ should be non-overlapping as Fig. 2(b) to eliminate short-circuit

loss. Based on the previous analysis, an improved design and its clock scheme are presented and shown in Fig. 2.

In Fig. 2, to form the gate driver circuits, four extra CMOS transistors and two extra capacitors are added. In the proposed circuit, two auxiliary clock signals (CK_A and CK_B) are connected to two small auxiliary capacitors (C_1 and C_2). In the case of this charge pumps, there are three kinds of operation modes. In the first operation mode shown in Fig. 2(a), CK_B and CK_2 are high, CK_A and CK_1 are low, C_1 and C_{p1} will be charged into the power supply voltage. C_{p2} is series with the voltage of CK_2 and the voltage V_2 will be transferred to the output node. In the second operation mode shown in Fig. 2(b), CK_A and CK_B are low, CK_1 and CK_2 are high, C_{p1} and C_{p2} are series with the voltage of $CK_{1,2}$ and the voltage $V_{1,2}$ will be transferred to the output node. In the third operation mode shown in Fig. 2(c), CK_A and CK_1 are high, CK_B and CK_2 are low, C_2 and C_{p2} will be charged into the power supply voltage. C_{p1} is series with the voltage of CK_1 and the voltage V_1 will be transferred to the output node. In order to avoid any breakdown issues, the voltages V_{gs}, V_{gd} and V_{ds} of the transistors must not exceed VDD. In the worst case where V_{IN} is equal to VDD and the output is unloaded, both gate drive signals must swing within a range from VDD to $2VDD$ to turn on or turn off M_{p1} and M_{p2}. If charge pumps are cascaded to be an n-stage charge pump, the drive signals in the nth stage should swing from $nVDD$ to $(n+1)VDD$. Therefore, the phase shifting circuit in [4] cannot turn on and turn off the nth stage CMOS transistors because the voltage range of the phase shifting circuit is from 0 to $nVDD$, and an excessive voltage can destroy the oxide layer of CMOS transistors. Adding two auxiliary clock signals (CK_A, CK_B) connected to two small auxiliary capacitors to turn on and turn off the nth stage CMOS transistors, We can keep the gate voltage swing in the range of nV_{IN} to $(n+1)V_{IN}$. In the circuit shown in Fig. 2, when CK_A is high, M_{n3} and M_{n4} are turned on, the voltage of the input terminal will be charged to C_2 and C_{p2}, and the gate voltage of M_{p1} changes from V_{IN} to $2V_{IN}$. Similarly, when CK_B is high, the gate

voltage of M_{p2} changes from V_{IN} to $2V_{IN}$. Even in an n-stage charge pump, the gate voltage of the nth stage PMOS transistor is maintained in the range from nV_{IN} to $(n + 1) V_{IN}$, eliminating the voltage overstress problem.

From the Fig. 2(d), we can see that we can make sure PMOS transistors can be turned off before the CK_1 goes low and NMOS transistors will be turned off before the CK_1 goes high. The PMOS transistors and NMOS transistors will not be turned on at the same time. Therefore, the reversion loss of the charge pump has been eliminated.

The single-stage charge pump can be cascaded to obtain a higher output voltage. As a result, a single-stage charge pump without load can provide an output voltage of $2VDD$. Multiple single-stage cross coupled circuits can be cascaded to obtain a high output voltage, ideally, the n-stage gate cross coupled circuit can get an output voltage of $(n + 1) V_{IN}$. In [3] a multi-stage gate-coupled charge pump circuit is proposed. That circuit does not consider the reversion loss and the substrate effect. The output voltage is lower than the ideal voltage, and the power conversion efficiency is very low. The reversion charge consumption problem is analyzed. However, with the increase of the stage, the source voltage of NMOS transistors is increasing and the substrate effect seriously affects the efficiency of the charge pump.
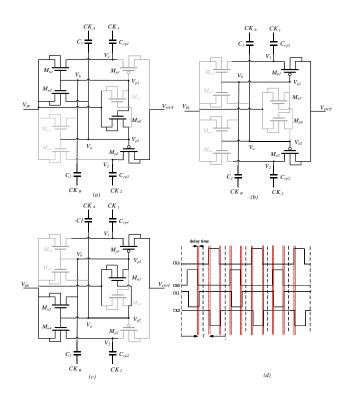

Fig. 2. The operation of the proposed four phase cross-coupled charge pump

IV. SIMULATION RESULTS

The proposed charge pump was simulated in 0.18μm CMOS technology. In the proposed design, both of the flying capacitors and the output capacitor are 30pF. The two auxiliary capacitors are 2pF. Simulation results of the circuit were compared with that of [3]. In order to ensure a fair comparison of the proposed design to other designs, all of the flying capacitors, output capacitors and the transferring switches in these designs are chosen with the same specifications. Fig. 3 shows that the output voltage of a 3-stage cross-coupled charge pump is 5.98V, in the no-load condition, when the input voltage VDD is equal to 1.5V. The maximum voltage conversion efficiency is equal to 99.8%.
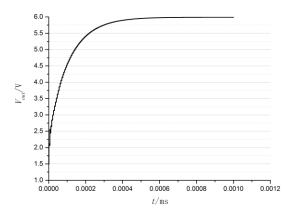
Fig. 3. Simulation output voltage of the proposed three stage charge pump

In Fig. 4, the output voltages of the proposed design and another design with different load are compared. The proposed design works better than the other design when the load is larger than 2kΩ. The auxiliary charge circuit is reduced or eliminated because these additional auxiliary circuits consume power and will reduce the conversion efficiency of the charge pump circuit and reduce the stability of these circuits [6-7].
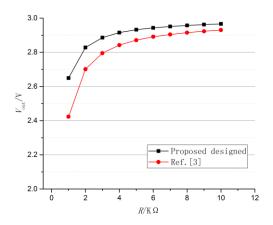

Fig. 4. Output voltage comparison of different single stage charge pump

designs with different loads

Fig. 5 shows the output voltage of different charge pumps when the load resistance is equal to 100KΩ and the input voltage changes from 0.8V to 1.8V. Under high load conditions, the difference of output voltage between these two charge pumps is small.
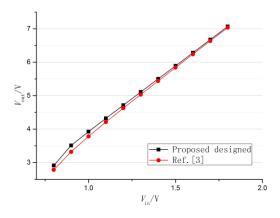

Fig. 5. The relation between the input voltage and the output voltage

In Fig. 6, the new charge pump is compared with the circuit in [3] with a load current of 56.21uA. The ripple voltage of the new charge pump is significantly smaller than that of the conventional cross-coupled charge pump proposed in [3].
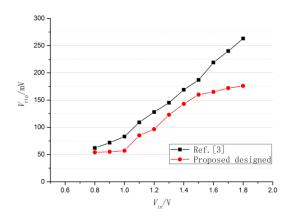

Fig. 6. Output ripple voltage comparison of different 3-stage charge pumps

with different V_{IN}

What's more, the proposed three-stage voltage charge pump performs much better in the PE (power efficiency) due to the elimination of the reversion power loss. The peak efficiency of this work and [3] are around 81.2% and 69.3%, and

the power consumption of this work, and [3] are 35mW and 66mW, respectively.

V. CONCLUSIONS

This paper has presented a new charge pump circuit with a new control method. The proposed structure eliminates all reversion power losses by using four non-overlapping clock signals and small auxiliary capacitors. The simulation results show that we can get a higher output voltage and a low ripple voltage compared to some published results. What's more, this design does not require any extra level shifter circuit and both of the gate-to-source/drain voltage and drain-to-source voltage do not exceed the nominal supply voltage.

VI. ACKNOWLEDGMENTS

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