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A 0.1-5.0 GHz Flexible SDR Receiver with Digitally Assisted Calibration in 65nm CMOS

Xinwang Zhang, Zipeng Chen, Yanqiang Gao, Yang Xu, Bingqiao Liu, Qian Yu, Yichuang Sun, Zhihua Wang, Baoyong Chi

Abstract—A 0.1-5.0 GHz flexible software-defined radio (SDR) receiver with digitally assisted calibration is presented, employing a zero-IF/low-IF reconfigurable architecture for both wideband and narrowband applications. The receiver composes of a main-path based on a current-mode mixer for low noise, a high linearity sub-path based on a voltage-mode passive mixer for out-of-band rejection, and a harmonic rejection (HR) path with vector gain calibration. A dual feedback LNA with “8” shape nested inductor structure, a cascode inverter-based TCA with miller feedback compensation, and a class-AB full differential Op-Amp with Miller feed-forward compensation and QFG technique are proposed. Digitally assisted calibration methods for HR, IIP2 and image rejection (IR) are presented to maintain high performance over PVT variations. The presented receiver is implemented in 65nm CMOS with 5.4mm² core area, consuming 9.6-47.4mA current under 1.2V supply. The receiver main path is measured with +5dBm/+5dBm IB-IIP3/OB-IIP3 and +61dBm IIP2. The sub-path achieves +10dBm/+18dBm IB-IIP3/OB-IIP3 and +62dBm IIP2, as well as 10dB RF filtering rejection at 10 MHz offset. The HR-path reaches +13dBm/+14dBm IB-IIP3/OB-IIP3 and 62/66dB 3rd/5th-order harmonic rejection with 30-40dB improvement by the calibration. The measured sensitivity satisfies the requirements of DVB-H, LTE, 802.11g, and ZigBee.

Index Terms—Wireless receiver, Soft-defined radio, low noise amplifier, Digitally-assisted calibration, RF, CMOS

I. INTRODUCTION

With the rapid development of wireless communication, there has been great demands for software-defined radio (SDR) receivers that can support multiple different wireless communication standards within a single chip. Most of the reported SDR receivers [1, 2] adopt the reconfigurable zero-IF architecture to support wideband modulation for public cellular applications. Meanwhile, there are other wireless connectivity applications with narrow bandwidth, such as the GSM and ZigBee, for which the low-IF receiver is more suitable [3]. This work presents a 0.1-5.0 GHz flexible SDR receiver [4] with a zero-IF/low-IF reconfigurable architecture to support both wideband and narrowband applications, covering from 5KHz to 20MHz. It is preferred to reconfigure the receiver into

zero-IF architecture, except that the signal bandwidth is narrow or the signal power is concentrated in close-to-DC frequencies. In these cases, a great part of the useful signal power would be filtered out by the embedded high-pass DC-offset cancellation loop (DCOC) in the analog baseband if the receiver is still reconfigured into zero-IF architecture, which would increase the bit-error rate (BER) of the receiver. Instead, the low-IF architecture is used, with slightly higher power consumption and more image interferences.

A true SDR receiver should be reconfigurable to accommodate various application environments, especially with interferences. Wideband RF front-ends are widely used in reported SDR receivers. However, due to the lack of selective filtering, out-of-band blockers and harmonic interferences are amplified in the same way as the desired signal, leading to significant SNR degradation. Recently, receivers [2] based on the voltage-mode passive-mixer introduces high-Q RF filtering to suppress out-of-band blockers, without touching the harmonic interferences. To reject the harmonic interferences, the harmonic rejection (HR) mixer is needed, but gain and phase mismatch degrades the harmonic rejection ratio. Gain and phase mismatch calibration can be adopted to achieve high 3rd-order harmonic rejection (HR3) and 5th-order harmonic rejection (HR5) [5]. However, the calibration procedure is complicated as the gain and phase mismatches are calibrated simultaneously. In [6], two-stage 8 phase HR mixer is adopted to reduce gain mismatch, and dynamic transmission gate technique is used to reduce phase mismatch. Therefore, high HR3 and HR5 are achieved without calibration. However, these techniques consume higher power consumption compare with the conventional HR mixer technique.

In this work, three reconfigurable flexible RF front-end paths (HR/main/sub path) are employed to achieve low noise, high linearity and harmonic rejection. For the HR path (0.1-1.5 GHz), the harmonic rejection mixer with vector calibration mechanism is used to reject harmonic interferences, while for the high-band (1-5 GHz) operation, a LC tuned low noise amplifier (LNA) in the main path provides the RF band-pass filtering to reject the harmonic interferences effectively, while a sub-path achieves high linearity with high-Q RF band-pass filtering to reject the out-of-band blockers. As the first stage of the receiver, the LNA should tolerate strong blockers besides low noise figure (NF). Traditional wideband LNA [7] is not suitable for the SDR application, as it amplifies both desired signals and blockers simultaneously. A high-linearity LNA [2]

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was proposed to handle the blockers up to 0dBm at the cost of a dedicated high-voltage supply. In this paper, a dual feedback LNA is proposed to increase the linearity and reduce NF.

Power consumption is another important specification for the SDR receiver, and the power consumption of the analog baseband as well as ADC is an important part, which is mainly consumed by the embedded Op-Amps. So the Op-Amp must trade-off between the power consumption and the performance. Two important merits are high frequency performance and the driving capacity. The bandwidth expansion technique in [8] is proposed to improve the Op-Amp bandwidth performance, with a cross-connected capacitor as a negative capacitor. However, this introduces a notch in the phase-frequency response, deteriorating the stability of the Op-Amp. The class-AB output stage is widely used for heavy loading and high linearity. But a conventional class-AB output stage needs a feedback loop [9], which increases the power dissipation and circuit complexity. In this work, the power-scalable class-AB full differential Op-Amp with Miller feed-forward compensation and quasi-floating gate (QFG) technique is proposed to achieve both high linearity and low power.

In previous work, calibrations such as the HR [10], second-order intermodulation intercept point (IIP2) [10] and I/Q mismatch [11] are realized manually, which is inefficient, inconvenient and costly. Most of them interrupt the receiver's normal operation. In this paper, digitally assisted calibrations are proposed for the SDR receiver. As digital circuits are more robust against process, voltage and temperature (PVT) variations, the digitally-assisted calibration is an optimized method to maintain the receiver performances in different application environments.

The work combines a lot of design techniques to implement a highly integrated SDR receiver and achieve superior performance. Compared to [4], this paper is extended in the way of further investigating the research background, discussing the technique to reject out-of-blockers and harmonic interferences with theoretical analysis, detailing circuit descriptions for key blocks, as well as introducing the digitally-assisted self-calibration. More measured results are shown to evaluate the complete performances in detail. The HR path is the same with [27]. However, the HR calibration is manual in [27] while the HR calibrations are automatically executed in a digitally assisted closed-loop form.

This paper is organized as following. Section II introduces the flexible receiver architecture, as well as considerations for the out-of-band blocker and harmonic interference. Section III describes the reconfigurable high linearity LNA. The down-conversion system of the main path is introduced in Section IV. Analog baseband circuits and reconfigurable continuous-time low pass (LP) and complex band pass (CBP) sigma-delta ADC is described in Section V. And digitally assisted calibration is introduced in Section VI. Finally, measured results are given in Section VII, followed by the conclusion in Section VIII.

II. SYSTEM ARCHITECTURE

A. Flexible Receiver Architecture

The architecture of the SDR receiver with three RF front-end paths is depicted in Fig. 1. The low NF main path embodies a differential high band frequency tunable LNA, one transconductance amplifier (TCA) and one current-mode passive mixer. The tunable LC tank in the LNA helps reject the out-of-band blockers and harmonic interferences. The high linearity sub-path consists of a voltage-mode passive mixer and a TCA, where a high-Q band-pass RF filter centered around the LO frequency is formed based on the passive mixer impedance transform principle to reject the out-of-band blockers. The HR path includes one wideband single-ended input differential output shunt-shunt feedback low band LNA, three TCAs with 5:7:5 transconductance ratio and an 8-phase current harmonic-rejection passive mixer with calibration mechanism to reject the 3rd/5th-order harmonic interferences. Since the linearity of the HR path is much higher than the main path, no additional high linearity sub-path is needed for the low band operation.

In the voltage-mode passive down-conversion, the TCA's low-pass input impedance can be transformed into bandpass that centered at LO frequency, which behaves as a high-Q bandpass filter at radio frequency. Therefore, the out-of-band blockers can be effectively rejected, which enables high linearity in the corresponding sub-path. As the prior TCA stage features low noise figure, the current-mode passive mixing is preferred for the low noise main-path. Outputs of the three RF front-end paths are summed up and filtered by a shared Tow-Thomas 2nd-order transimpedance amplifier (TIA).

A hybrid method is adopted to generate 8-phase LOs for the HR path. In the frequency band of 0.1-0.75GHz, 8-phase LOs are generated by two cascaded divided-by-2 circuits; in the frequency band of 0.75-1.5GHz, one divided-by-2 circuit generates the quadrature LOs and one phase rotator combines 0°/90°/180°/270° LOs to generate 45°/135°/225°/315° LOs based on the vector summing principle. For the 1-5GHz main path and sub-path, a LO generator generates the 25% duty-cycle LOs to drive the passive mixers.

Due to high resolution, wide bandwidth, inherent anti-aliasing filtering capability and potential for low power consumption, the SDR receiver adopts continuous-time (CT) Sigma-Delta (Σ - Δ) ADC to realize the analog-digital conversion, which provides inherent low-pass (LP)/complex band-pass (CBP) anti-alias filtering and high dynamic range, so that the requirements on the LP/CBP analog filter and programmable gain amplifier (PGA) are relaxed, thus lowering the power consumption. To maintain high performance over the PVT variations, the HR calibration, IIP2 calibration and I/Q calibration are used, and filter frequency tuner, DC-offset cancellation loop and automatic gain control (AGC) are also implemented with the digitally assisted calibration.

B. Out-of-Band Blockers

In this work, two solutions are proposed to make the receiver tolerate strong blockers, as shown in Fig. 2. Firstly, through

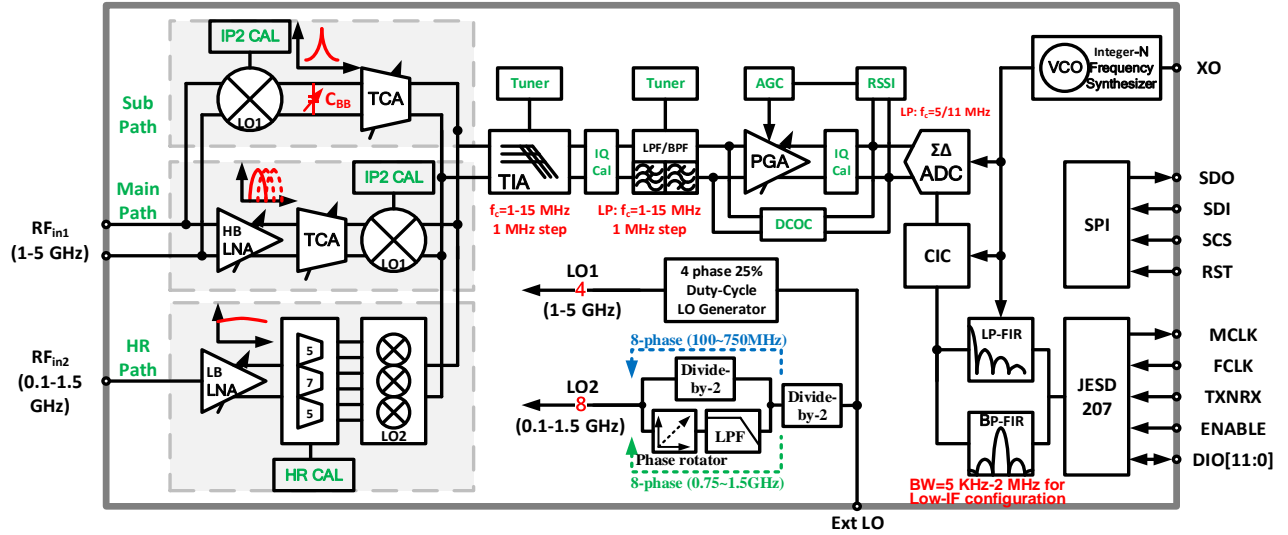


Fig. 1 The architecture of the presented SDR receiver

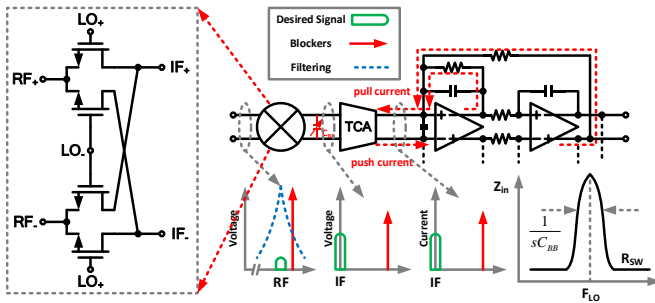


Fig. 2 Operation principle of the sub path in the presence of blockers

passive impedance translation [12], high-Q RF band-pass filtering occurs in the sub path. The parallel capacitor C_{BB} controls the bandwidth of the RF filter, and the out-of-band impedance is set by the passive mixer switch resistance R_{SW} . With the help of the RF filtering, the out-of-band blockers can be rejected to avoid saturating the TCA. Any residual blockers are removed by the following 2nd-order low-pass TIA.

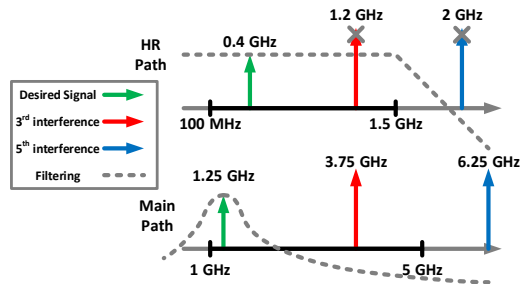


Fig. 3 Harmonic rejection methods of the HR path and main path

Ideally, the TIA presents low input impedance to prior stages, leading to low distortion. In reality, the TIA exhibits limited rejection on the out-of-band blockers, due to the limited gain-bandwidth product (GBW) and driving capability of the employed Op-Amps [13]. The residual blockers significantly deteriorate the receiver linearity and may saturate the following analog baseband circuits. So the embedded Op-Amps should

have wide enough GBW as well as strong driving capability. The first requirement is obvious, and the second requirement is explained as follows. As shown in Fig. 2, the strong blocker leads to large pull/push current, which affects the operation of the Op-Amps and deteriorates the TIA linearity. Class-AB output stage could provide large transient current in the occurrence of strong blocker. In this paper, the power-scalable class-AB Op-Amp with Miller feed-forward compensation and QFG technique is used to improve the linearity of the TIA.

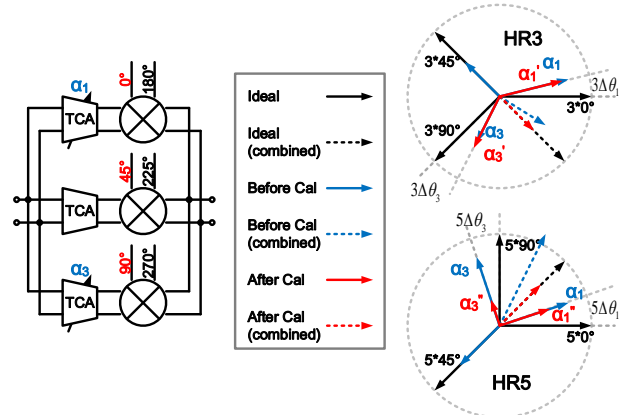


Fig. 4 Vector phase diagram of the HR3/5 before and after the calibration

C. Harmonic Interferences

Due to the higher linearity and lower $1/f$ noise compared to the active mixer, the passive mixer is suitable for recent SDR receivers. However, the passive mixer down-converts not only the desired signal but also interference signals around LO harmonics. As shown in Fig. 3, in this work, 0.1-5.0 GHz operation band is divided into two parts. The low-band (0.1-1.5 GHz) and high-band (1.0 GHz-5.0 GHz) receivers use a harmonic rejection mixer and a tunable 2nd-order band-pass filter to reject harmonic interferences, respectively.

Due to phase and gain mismatch, the harmonic rejection is limited to only 30-40dBc, which may not be sufficient to meet the system requirement [14]. Conventional calibration method [5] is complicated since the gain and phase need to be calibrated

simultaneously. In this work, HR calibration method [10] is adopted in the current-mode mixing, where only the gain calibration is necessary to compensate for mismatch.

As shown in Fig. 4, by including the phase error $\Delta\theta_1/\Delta\theta_3$ and gain error α_1/α_3 of the $0^\circ/90^\circ$ path, the 3rd-order harmonic of the three paths ($0^\circ/45^\circ/90^\circ$) are as follows:

$$f_0(t) = A\alpha_1 \cos(3\omega t + 3(0 + \Delta\theta_1)) \quad (1)$$

$$f_{45}(t) = \sqrt{2}A \cos\left(3\omega t + 3\frac{\pi}{4}\right) \quad (2)$$

$$f_{90}(t) = A\alpha_3 \cos\left(3\omega t + 3\left(\frac{\pi}{2} + \Delta\theta_3\right)\right) \quad (3)$$

In order to cancel the 3rd-order harmonic interference, the calibrated gains α_1/α_3 of the $0^\circ/90^\circ$ path can be adjusted as:

$$\alpha_1' \approx \frac{4 - 3\sin(\Delta\theta_3) - 3\cos(\Delta\theta_3)}{16 + 9\cos(\Delta\theta_1 - \Delta\theta_3) - 12\cos(\Delta\theta_1) - 12\cos(\Delta\theta_3)} \quad (4)$$

$$\alpha_3' \approx \frac{4 + 3\sin(\Delta\theta_1) - 3\cos(\Delta\theta_1)}{16 + 9\cos(\Delta\theta_1 - \Delta\theta_3) - 12\cos(\Delta\theta_1) - 12\cos(\Delta\theta_3)} \quad (5)$$

Therefore, for the 3rd-order harmonic rejection calibration, the ratio of the calibrated gains α_1'/α_3' of the $0^\circ/90^\circ$ path becomes:

$$\frac{\alpha_1'}{\alpha_3'} \approx \frac{4 - 3\sin(\Delta\theta_3) - 3\cos(\Delta\theta_3)}{4 + 3\sin(\Delta\theta_1) - 3\cos(\Delta\theta_1)} \quad (6)$$

Similarly, the 5th-order harmonic of the three paths are as follows:

$$f_0(t) = A\alpha_1 \cos(5\omega t + 5(0 + \Delta\theta_1)) \quad (7)$$

$$f_{45}(t) = \sqrt{2}A \cos\left(5\omega t + 5\frac{\pi}{4}\right) \quad (8)$$

$$f_{90}(t) = A\alpha_3 \cos\left(5\omega t + 5\left(\frac{\pi}{2} + \Delta\theta_3\right)\right) \quad (9)$$

In order to cancel the 5th-order harmonic interference, the calibrated gain α_1''/α_3'' of the $0^\circ/90^\circ$ path can be adjusted as:

$$\alpha_1'' \approx \frac{4 - 5\sin(\Delta\theta_3) - 5\cos(\Delta\theta_3)}{-16 - 25\cos(\Delta\theta_1 - \Delta\theta_3) + 20\cos(\Delta\theta_1) + 20\cos(\Delta\theta_3)} \quad (10)$$

$$\alpha_3'' \approx \frac{4 + 5\sin(\Delta\theta_1) - 5\cos(\Delta\theta_1)}{-16 - 25\cos(\Delta\theta_1 - \Delta\theta_3) + 20\cos(\Delta\theta_1) + 20\cos(\Delta\theta_3)} \quad (11)$$

Therefore, for the 5th-order harmonic rejection calibration, the ratio of the calibrated gain α_1''/α_3'' of the $0^\circ/90^\circ$ path is given by:

$$\frac{\alpha_1''}{\alpha_3''} \approx \frac{4 - 5\sin(\Delta\theta_3) - 5\cos(\Delta\theta_3)}{4 + 5\sin(\Delta\theta_1) - 5\cos(\Delta\theta_1)} \quad (12)$$

In the presented approach, the HR3 and HR5 cannot be optimized at the same time. Generally, the HR3 is more important than the HR5 since the 5th-order harmonic is further away than the 3rd-order harmonic, so the calibration is carried out to optimum the HR3 in most cases. However, the calibration may not optimize HR5 if there are strong interferences at the 5th-order harmonic frequency. In the case that both HR3 and HR5 are important, the calibration would be performed with an one-by-one search algorithm to find the code which makes HR3 and HR5 higher than the required value. Even though HR3 and HR5 are not the best in this case, the harmonic rejection can be high enough to meet the specification.

Since the calibration codes are only 6 bits, there is no speed issue to run the algorithm.

III. RECONFIGURABLE HIGH LINEARITY LNA

A. Dual Feedback LNA

Fig. 5 (a) shows the conventional common-gate LNA (CGLNA), of which the inductor resonates with the parasitic capacitor at input. It is very suitable for wideband receiver, but its NF is limited to $1+(\gamma/\alpha)$ when the input impedance is matched. Therefore, the conventional CGLNA has a trade-off between noise and input matching. To address this issue, the capacitive cross-coupled CGLNA [15] is proposed, based on a single feedback structure (Fig. 5 (b)). The g_m -boosting with the inverting amplification (A_2) reduces the thermal noise contribution of M_1 by a factor of $1+A_2$ under input impedance matching condition. The drawback of single feedback is that the inverting amplification provided by the passive g_m -boosting is less than 1. In this paper, dual feedback CGLNA (Fig. 5 (c)) with passive components is proposed to reduce noise figure with two feedback stages A_1 and A_2 . Besides, the presented LNA could provide the RF band-pass filtering to effectively reject the harmonic interferences, compared with other wideband dual-feedback CGLNAs [33, 34]. The main properties of the feedback based CGLNA topologies are summarized in TABLE I.

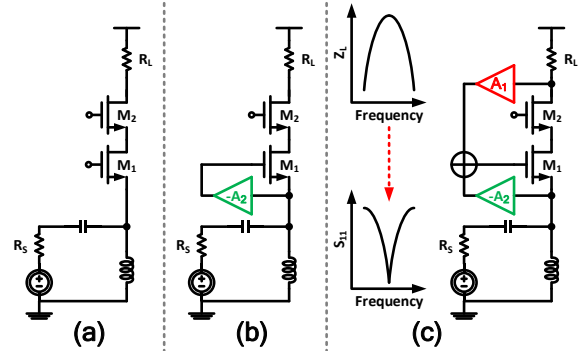


Fig. 5 (a) Conventional CGLNA, (b) Single feedback CGLNA, (c) Dual feedback CGLNA

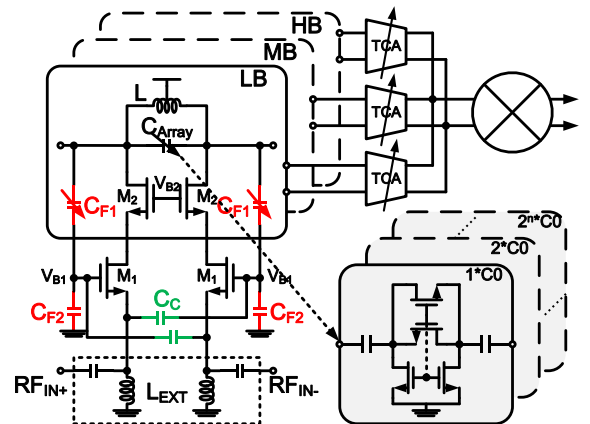


Fig. 6 Schematic of the dual feedback LNA

The model of the dual feedback LNA is shown in Fig. 5 (c). Feedback loop A_1 tunes the input stage simply by means of the load Z_L , and feedback loop A_2 increases the g_m of the input

transistor to reduce the power consumption. The schematic of the dual feedback LNA is shown in Fig. 6. Capacitors C_{F1} and C_{F2} form the voltage-voltage feedback A_1 , and capacitor C_C

forms the feedback A_2 . The tunable LC resonant loads are adopted to achieve low noise and high linearity. The input impedance of the proposed LNA is given by:

TABLE I

MAIN PROPERTIES OF THE FEEDBACK CGLNA TOPOLOGIES

	Conventional CGLNA	Single feedback CGLNA	Dual feedback CGLNA
A_v	$\frac{R_L}{2R_S}$	$\frac{R_L}{2R_S}$	$\frac{R_L}{2R_S}$
Z_{in}	$\frac{1}{g_{m1}}$	$\frac{1}{g_{m1}(1+A_2)}$	$\frac{1}{g_{m1}(1+A_2)} + \frac{A_1 R_L}{1+A_2}$
F^*	$1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L}$	$1 + \frac{\gamma}{\alpha(1+A_2)} + \frac{4R_S}{R_L}$	$1 + \frac{\gamma}{\alpha(1+A_2)(1+A_1 g_{m1} R_L)} + \frac{4R_S}{R_L}$

* Thermal noise due to M_2 is negligible and is not shown in the equation

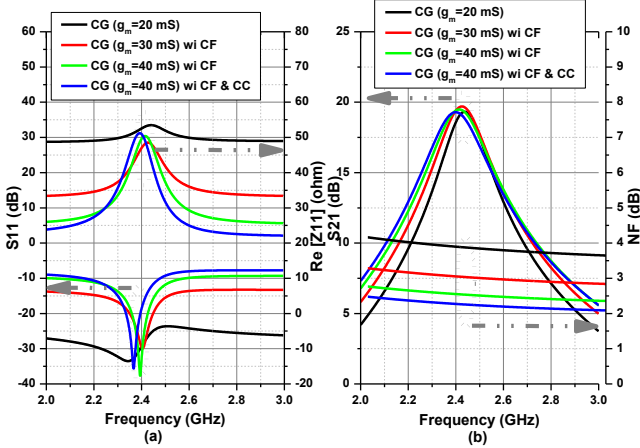


Fig. 7 Simulated results of (a) S_{11} and $\text{Re}[Z_{11}]$, (b) S_{21} and NF of the HBLNA

$$Z_{in}(j\omega) = \frac{1}{g_{m1}(1+A_2)} + \frac{A_1 Z_L(j\omega)}{1+A_2} \quad (13)$$

where, $A_1 \approx C_{F1}/(C_{F1}+C_{F2})$, $A_2 \approx C_C/(C_C+C_{F1})$, assuming $C_{gs} \ll C_{F1}, C_{F2}, C_C$. The input impedance is purely resistive at the load resonance frequency. Fig. 7(a) shows the simulated S_{11} and $\text{Re}[Z_{11}]$ when the LNA is configured to work at 2.4GHz, and the performances at other frequency points are similar. As g_m increases, Z_L holds more of Z_{in} . And the input matching network provides more rejection for the out-of-band blockers. Besides, with the capacitor C_C , g_m is almost doubled.

The noise factor F of the proposed LNA is given by a sum of contributions as in (14):

$$F = 1 + \frac{\gamma}{\alpha(1+A_2)(1+A_1 g_{m1} R_L)} + \frac{4R_S}{R_L} \quad (14)$$

where γ and α are bias-dependent parameters[16]. Compared with the conventional CG LNA, the noise contribution of M_1 is reduced by $(1+A_2)(1+A_1 g_{m1} R_L)$. As shown in Fig. 7(b), with the help of the dual feedback A_1 and A_2 loops, the proposed LNA lowers down the NF by about 1.5dB, compared to the conventional CG LNA.

As the input node of the CG LNA is low impedance node and the LC load supports larger voltage swing, the proposed LNA features higher in-band linearity, compared with the conventional CG wideband LNA with the resistive load. As both the input matching (S_{11}) and the gain (S_{21}) feature out-of-band rejection, as shown in Fig. 7, the proposed LNA

features higher out-of-band linearity. Therefore, the proposed dual feedback LNA has higher linearity.

B. "8" Shape Nested Inductor

To cover 1-5GHz wide frequency band, the LNA uses three resonant loads with three inductors. Only one of them is active at a time. The cascode transistor M_2 in Fig. 6 works as switch to turn off another two inductors. The tuning ranges of three tanks are 1.0-1.9GHz, 1.9-3.3GHz, 3.3-5GHz. And there is

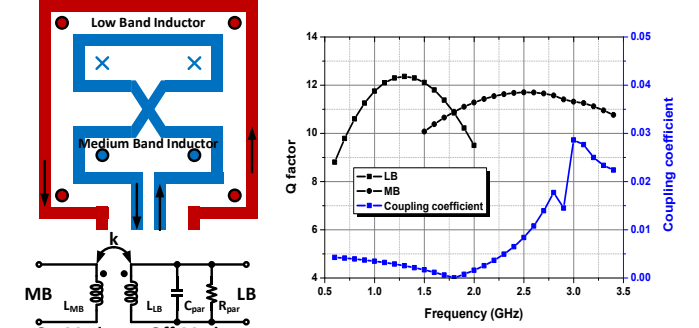


Fig. 8 "8" shape inductors and simulated results of Q factor and coupling coefficient

about 100MHz overlaps between LC tanks. As three inductors occupy large area, the stack inductor and nested inductor structure are proposed. The stack inductor structure[17] realizes multiple inductors using different metal layers and occupies the same area of one inductor. However, these inductors have different quality factor. The nested inductor structure[18] consists of outer and inner diameter inductors. But it features poor isolation between them. In this work, high-band inductor adopts normal inductor, while low-band (LB) and medium-band (MB) inductors are placed into one nested structure to save the die area, as shown in Fig. 8. Simulation shows that the performance difference between the "8" shape nested inductor and the normal inductor is small, and wouldn't degrade the LNA performance. However, the off-mode inductor can introduce parasitic capacitance C_{par} and parasitic resistance R_{par} , which can affect the equivalent inductance of the on-mode inductor [19]. Therefore, the coupling coefficient (k) should be kept small. In order to reduce the coupling between these two inductors, the "8" shape nested structure [20] is utilized. The simulated results with HFSS show that the coupling coefficient between the LB inductor and the MB inductor is below 0.029.

C. Wideband Shunt-Shunt Feedback LNA

A wideband shunt-shunt active feedback single-ended LNA [35, 36] is used in the HR path. The current bleeding technique [37] is adopted to increase the drain-to-source voltage swing of the amplified transistor with the improved linearity. A high linearity active balun with a source-degenerated common-source transistor is used to realize the singled-ended-to-differential conversion. The presented single-ended LNA with on-chip active balun could save the power (the differential LNA would consume twice the power) and lower down the cost by avoiding the off-chip balun component.

IV. DOWN-CONVERSION SYSTEM IN MAIN PATH

The main path adopts the current-mode architecture with a cascode inverter-based TCA, a passive mixer and a flexible Tow-Thomas 2nd-order TIA. To reduce the conversion loss, a 25% (instead of 50%) duty-cycle LO generator, similar with [21], is used to generate the 25% duty-cycle LOs to drive the passive mixer. The LOs are driven to the rail-to-rail square wave with the inverter chain, which could increase the down-conversion performance (noise and conversion gain) at the cost of the power consumption.

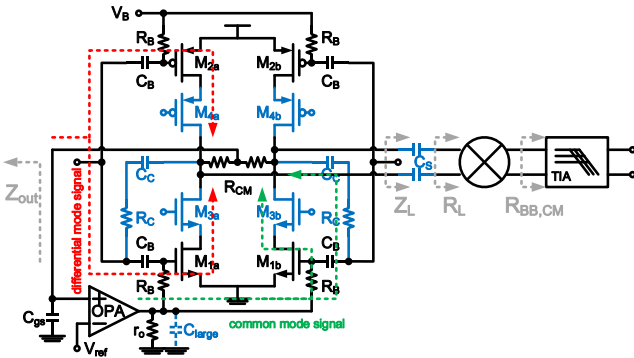


Fig. 9 Schematic of high isolation TCA with Miller compensation

A. High Isolation TCA with Miller Feedback Compensation

Traditionally, the inverter-based topology is usually adopted in the TCA design. However, the poor isolation makes the input impedance of the TCA dependent on the following stage impedance and causes gain fluctuation of the preceding LNA under various reconfigurations. In this paper, the cascode inverter-based topology is used [22], as shown in Fig. 9.

As the input impedance $R_{BB,CM}$ of the TIA varies greatly under different operation modes, and the load impedance R_L of the TCA is a function of $R_{BB,CM}$ [12]. According to (15), as the LO frequency increases, R_L changes accordingly, where Z_{sh} models overall loss of the passive mixer and the scaling factor γ is $2/\pi^2$. Moreover, for different operation modes, the output impedance of the preceding circuit Z_{out} changes. Besides, in order to block low frequency 2nd-order intermodulation (IM_2), the AC coupling capacitor C_S is needed. Therefore, these factors may lead to the unstable common-mode feedback loop for the TCA.

$$R_L = \begin{cases} R_{sw} + \gamma R_{BB,CM}, & \text{Low LO Frequency} \\ R_{sw} + \gamma R_{BB,CM} \parallel Z_{sh}, & \text{High LO Frequency} \end{cases} \quad (15)$$

TABLE II shows the poles and zeros of four TCA topologies, where g_{m1} and r_{o1} are the transconductance and output impedance of M_1 , g_m and r_o are the transconductance and output impedance of the Op-Amp (OPA). From the second column, it can be seen that the output impedance of the former circuit Z_{out} decides the zero position. So the common-mode stability of the TCA should consider the former circuit. As shown in Fig. 10, with the coupling capacitor C_S , phase margin (PM) is decreased from 60.6° to 46.7° , due to high input impedance of the next stage at low frequency. In order to increase the TCA common-mode PM, a big capacitor C_{large} is inserted [23]. For the PM to be larger than 60° , C_{large} needs to be 15pF, which requires large chip area.

In this work, Miller feedback compensation with R_C and C_C is utilized to maintain common-mode loop stability. As shown in Fig. 9, for high frequency differential signal, the resistor R_C is larger than low input impedance of the following stage (TIA). Therefore, the capacitor C_C and resistor R_C path is nearly open, and the differential bandwidth is not affected. From the fifth column of TABLE II, an additional zero is added, comparing with the big capacitor C_{large} case. So the phase margin is improved. As shown in Fig. 10, only 200fF C_C and 10k Ω R_C are needed to obtain 60° phase margin.

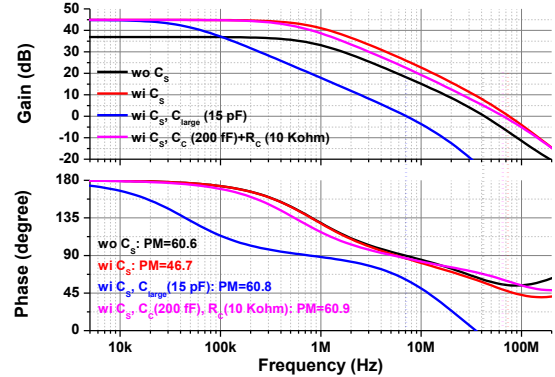


Fig. 10 Simulated common-mode PM results of four TCAs

B. Op-Amp with Miller Feed-Forward Compensation and QFG Technique

The linearity of the TIA is dependent on the GBW and the driving capability of the embedded Op-Amp (Fig. 11). To trade-off performance and power consumption, the Op-Amp consists of four G_m units, and each G_m unit also includes four class-AB output stage arrays. Resistor R_F is introduced with capacitor C_F to realize nulling-resistor Miller feed-forward (NRMFF) compensation to enhance all of bandwidth, GBW and phase margin. Although the C_F/R_F path introduces positive feedback, the stability of the amplifier could be guaranteed by properly setting the feedback depth of the C_F/R_F and C_C/R_C paths. A class-AB output stage with resistor R_E and capacitor C_E is proposed with the so-called QFG technique [24]. And resistor R_E is implemented by a diode-connected sub-threshold MOS transistor. In order to avoid large voltage drop owing to

leakage current, M4 adopts thick oxide gate transistor. To improve the stability of the common mode feedback loop, the resistor R_M and capacitor C_M are added to contribute the passive left half plane (LHP) zero. Assuming $g_{m1}R_1 \gg 1$, $g_{m2}R_2 \gg 1$, $C_2, C_C, C_F, C_E \gg C_1$, $R_E \gg R_1, R_2, R_C, R_F$, extensive analysis of the proposed circuit yields:

$$z_1 \approx -\frac{1}{R_F C_F + R_C C_C + R_E C_E} \quad (16)$$

$$z_2 \approx -\frac{1}{R_C C_C + R_F C_F}, z_3 \approx -\frac{1}{R_F C_F} - \frac{1}{R_C C_C} \quad (17)$$

$$p_1 \approx -\frac{1}{g_{m2} R_2 R_1 (C_C - C_F) + R_E C_E} \quad (18)$$

$$p_2 \approx -\frac{1}{g_{m2} R_1 R_2 (C_C - C_F)} - \frac{1}{R_E C_E} \quad (19)$$

$$p_3 \approx -\frac{g_{m2} (C_C - C_F)}{C_C C_F [4 - g_{m2} (R_C - R_F)]} \quad (20)$$

$$p_4 \approx -\frac{R_1 [4 - g_{m2} (R_C - R_F)]}{(R_1 R_F + R_1 R_C + R_C R_F) C_L} \quad (21)$$

$$p_5 \approx -\frac{1}{C_1} \left(\frac{1}{R_C} + \frac{1}{R_F} + \frac{1}{R_1} \right) \quad (22)$$

TABLE II
POLES AND ZEROS OF FOUR TCA TOPOLOGIES (Z_{out} AND Z_L PRESENT REAL IMPEDANCE)

	without C_S	with C_S	with C_S, C_{charge}	with C_S, R_C, C_C
z_1	$-\frac{1}{Z_{out} C_B}$	$-\frac{1}{Z_L C_S + Z_{out} C_B}$	$-\frac{1}{Z_L C_S + Z_{out} C_B}$	$-\frac{1}{R_C C_C}$
z_2		$-\frac{1}{Z_L C_S} - \frac{1}{Z_{out} C_B}$	$-\frac{1}{Z_L C_S} - \frac{1}{Z_{out} C_B}$	$-\frac{1}{Z_{out} C_B + Z_L C_S}$
z_3				$-\frac{1}{Z_{out} C_B} - \frac{1}{Z_L C_S}$
p_1	$-\frac{1}{R_B C_B}$	$-\frac{1}{R_B C_B + r_{o1} C_S}$	$-\frac{1}{R_B C_B + r_{o1} C_S + r_{o1} C_{charge}}$	$-\frac{1}{g_{m1} r_{o1} R_B C_C}$
p_2	$-\frac{2}{R_{CM} C_{gs}}$	$-\frac{1}{R_B C_B} - \frac{1}{r_{o1} C_S}$	$-\frac{1}{R_B C_B + r_{o1} C_S}$	$-\frac{1}{Z_{out} C_B + Z_L C_S + R_{CM} C_{gs}}$
p_3		$-\frac{2}{R_{CM} C_{gs}}$	$-\frac{1}{R_B C_B} - \frac{1}{r_{o1} C_S}$	$-\frac{Z_{out} C_B + Z_L C_S + R_{CM} C_{gs}}{Z_{out} Z_L C_B C_S + Z_{out} R_{CM} C_B C_{gs} + R_{CM} Z_L C_S C_{gs}}$
p_4			$-\frac{2}{R_{CM} C_{gs}}$	$-\frac{1}{R_{CM} C_{gs}} - \frac{1}{Z_L C_S} - \frac{1}{Z_{out} C_B}$

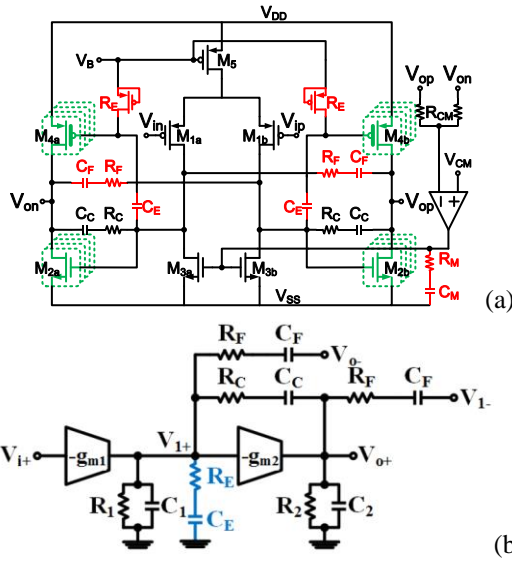


Fig. 11 (a) Schematic of the embedded Op-Amp [4]; (b) Differential-mode small signal equivalent circuit

where g_{m2} is the transconductance of the output stage, R_1 and R_2 are the output resistance of the input and output stages, respectively, C_L is the load of the Op-Amp, and $R_F \approx R_C$ is

assumed. From (16) and (18), as capacitor C_C equals C_F , the dominant zero is lower than the dominant pole, which boosts dc gain starting at the corner frequency $f_H = 1/(2\pi R_E C_E)$. Two non-dominant zeros (17) are used to cancel two non-dominant poles (19) and (20) by adjusting R_F and R_C . And another two non-dominant pole (21) and (22) are pushed to high frequency. Ultimately the complex two-stage Op-Amp becomes a single pole system. The simulated results show that with the NRMFF and QFG techniques, the BW/GBW of the Op-Amp increases from 2.5/264 MHz to 10.4/412 MHz, compared with the nulling-resistor Miller feedback (NRMFB) technique. As shown in Fig. 12, better out-of-band linearity of the TIA is achieved with the NRMFF and QFG techniques. And simulated results show that IP1dB and IIP3 of the TIA are improved by 13dB and 17dB, respectively.

V. ANALOG BASEBAND CIRCUITS AND RECONFIGURABLE CONTINUOUS-TIME LB/CBP SIGMA-DELTA ADC

To meet the channel selection requirement of most wireless communication standards, the SDR receiver uses the 5th-order filtering to relax the requirement on the ADC dynamic range [22]. Generally, the 5th-order IF analog filter consists of five operational amplifiers, which need large power consumption.

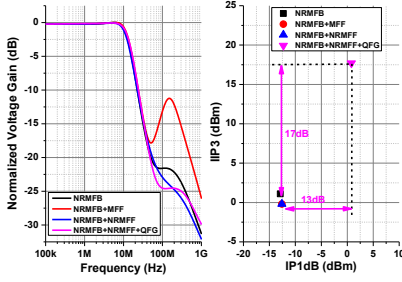


Fig. 12 Simulated transfer characteristic, IP1dB and IIP3 of the TIA

In this paper, the TIA features 2nd-order filtering, and the IF analog filter only offers 3rd-order filtering, which needs three operational amplifiers and reduces power consumption. Besides, the 2nd-order filtering TIA can reject some interferences and reduce the linearity requirement on the IF analog filter. Although gm-C filter can operate at higher frequencies than active RC filter, the linearity of gm-C filter is worse comparing to active RC filter. For the SDR receiver, high linearity IF analog filter is important to reject the interferences, this paper adopts 3rd-order active RC filter. Besides, the IF analog filter features LP/CBP reconfigurable structure, which is designed for the zero/low-IF architecture reconfigurable receiver.

Two PGAs further maximize the dynamic range with 36dB gain and a step size of 1dB. As the passive components' nominal values are subject to fabrication process, a filter tuning circuit is required to compensate for the variation of both the resistor and capacitor values. To calibrate the offset from the PGA, an active DC offset cancellation loop is adopted.

The amplified transistors in the analog baseband use PMOS and the transistor length is large, which could decrease the 1/f noise contribution effectively.

In order to trade-off power consumption and design complexity, the proposed CT Σ - Δ ADC can be reconfigured to either 5/11 MHz single-side BWs in LP mode or 5/10 MHz double-side BWs in CBP mode to support different applications [25]. For example, 5 MHz or 11 MHz single-side BW LP mode is adopted for 1.4/3/5/10 MHz or 15/20 MHz LTE standards, respectively. As shown in Fig. 13, it consists of an active-RC loop filter configured as a 3rd-order LP or 2nd-order CBP architecture, flexible switched current-steering DACs, and a 4-bit quantizer with the sampling frequency varying from 160 MHz to 320 MHz in different BWs. Feedforward compensation in integrators and digital calibrations, including DC trimming, RC trimming and comparators offset calibration, are adopted to improve the overall performance.

For LP mode, a hybrid 3rd-order loop filter combining feedback with local feedforward architecture is employed. The feedforward path with R_4 is utilized to eliminate one DAC normally used to feedback to the second integrator input. A local feedback path with R_Z is added to move one zero of the noise-transfer function away from DC to suppress the in-band quantization noise more sufficiently and therefore achieve higher SNR. Besides, to avoid the instability issue caused by excess loop delay, an additional feedback path is employed to

compensate for the stability of the modulator and the loop delay is set to half of the sampling period [26]. For CBP mode, a 2nd-order feedback complex loop filter is employed. It shares the first and third integrators and also the two connecting feedback DACs in LP mode. The cross-coupling path with RC is added to shift non-conjugate zeroes from DC to the center frequencies among different CBP modes. Because the 2nd-order CBP filter is unconditionally stable, the loop delay compensation path realized by the DAC3 and the fourth amplifier in LP mode are not necessary and also shut down to save power.

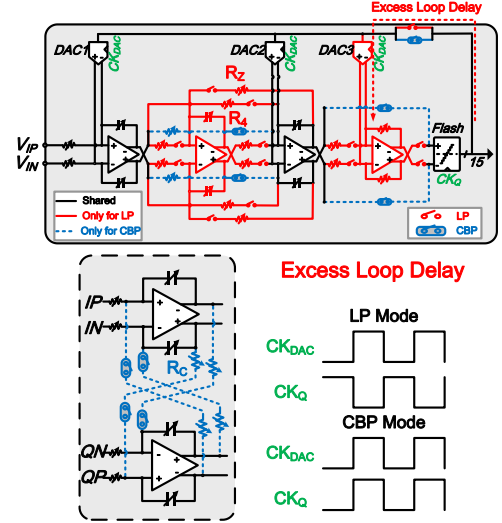


Fig. 13 Schematic of the CT LB/CBP Σ - Δ ADC

VI. DIGITALLY ASSISTED CALIBRATION

A. Architecture

The digitally assisted calibration has been implemented with the aid of one ADC (ADA-HSMC) and one FPGA (Altera DE2-115), as shown in Fig. 14. The RF test signal and LO signal are provided by two signal generators (Agilent E4438C, Agilent E8267D). In this loop, the I (or Q) path analog IF signal is sampled and digitalized by the 14-bit ADC. The FPGA senses the ADC output signal's power level, and provides the amplitude information. Then, the calibration algorithm is executed to generate the calibration signal to configure the receiver calibration circuits through the SPI control interface. In the practical transceiver, the loop-back test could be built to complete the calibration by injecting the transmitted signals into the receiver, without additional RF signal generator needed.

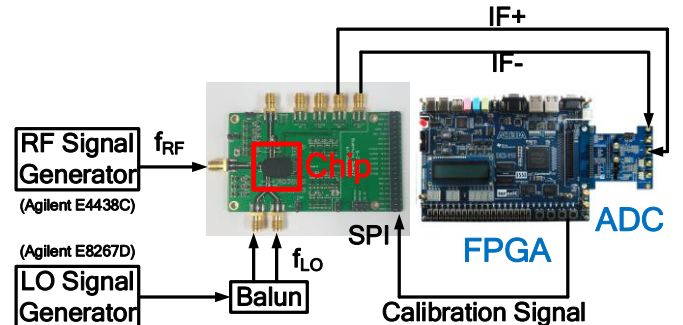


Fig. 14 Architecture of the digitally assisted calibration loop

As shown in Fig. 15, to calibrate the HR3 or HR5, one test tone ($f_{RF}=3*f_{LO}+5$ MHz or $f_{RF}=5*f_{LO}+5$ MHz) is applied to the receiver RF port. The gain adjustment of 0° path and 90° path is realized with variable gain TCA₁ and TCA₃ [27] in Fig. 15. With independent 2-dimensional gain calibration, optimized HR3 or HR5 can be achieved. For the IIP2 calibration, two test tones ($f_{RF1}=f_{LO}+100$ MHz and $f_{RF2}=f_{LO}+105$ MHz) are applied to the LNA input and a binary search algorithm is adopted to achieve the optimized IIP2. Differential current DAC in Fig. 15 tunes the gate voltages differentially to compensate the mismatch of the passive mixer switches [21]. Similarly, for the image rejection (IR) calibration, one test tone ($f_{RF}=f_{LO}-5$ MHz) is injected into the receiver RF port. I/Q mismatch calibration circuits based on the coefficient matrix method [28] are used, which calibrates the input I/Q signal of the complex bandpass filter. The calibration circuit works in the current mode domain, and the I/Q gain adjustment is realized by tuning the forward TCAs (Fig. 15). As the HR3/5, IIP2 and IR calibrations are operated in different circuits of the receiver, there is no conflict between all the calibrations.

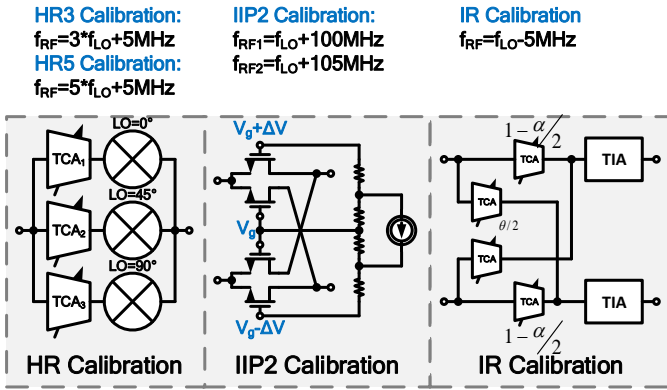


Fig. 15 The test tone of the HR, IIP2 and IR calibration

B. Algorithm

The digitally assisted calibration flow for IIP2, I/Q and HR is shown in Fig. 16. The initial signal source is located at $f_{LO}+f_{IF}$. The calibration starts from automatic gain control process, which adjusts the output of the PGA into the pre-determined range.

In the initial step, the power of the detected signal is detected by 2^9 times of accumulation. Then the control word is changed in one dimension/two directions (for IIP2 and I/Q calibration) or two dimension/four directions (for HR calibration). For the calibrations with only one dimension, a binary search algorithm is adopted to find the optimized control word, and the calibration is finished in only N cycles if the control word length is N bits. For calibrations with two dimensions, one dimension control word is swept while the other one kept fixed. Iterations will be performed between two dimensions until the optimum configuration is reached (usually 2~3 iterations are enough), and the convergence time is $k*(N1+N2)$ cycles (k is the iteration times (2~3), $N1$ and $N2$ are the control word length in two dimensions, respectively). The initial power is not the lowest, set the control word with the lowest power as the initial control word, and the next loop cycle will be repeated. The initial control word is always replaced by one that helps to get a

lowest detection power, which builds up the algorithm repeated loop cycle. After the calibration is finished, the calibration control word is fixed, the calibration algorithm is stopped and the receiver is switched into the normal receiving mode, which means that the calibration is executed only once and there is no drifting issue. Of course, the calibration should be executed again once the receiver operation environment (power supply or temperature) is changed.

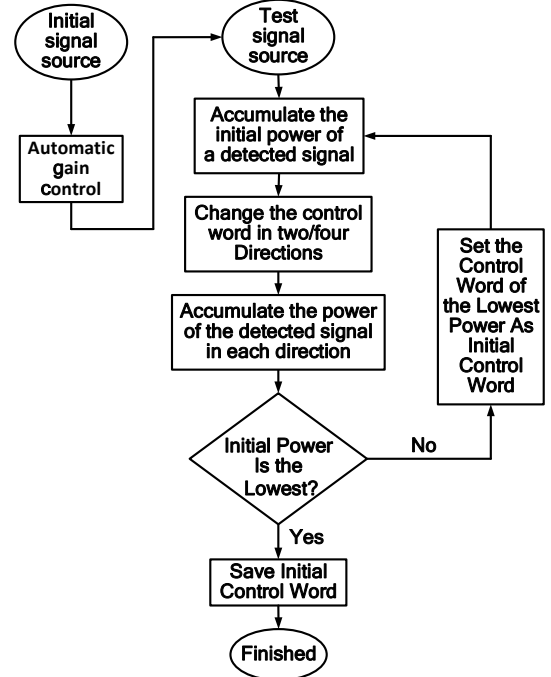


Fig. 16 Diagram of the digitally assisted calibration flow

C. Measured Results

Fig. 17 shows the measured main path IIP2 at 1/1.5/2.3 GHz with the digitally assisted calibration over 10 tests. An average of 60dBm is achieved with the presented calibration method. Fig. 18 shows the measured HR3/HR5 of the HR path at 100/700 MHz over 10 tests. With digitally assisted calibration, the HR3 and HR5 are around 57dB and 65dB, respectively. Fig. 19 shows the image rejection at 2-8 MHz center frequency over 10 tests. An average of 55dB is achieved with the auto calibration. The tuning resolution (tuning step) of the calibration unit in the circuit is the main limitation to the achievable calibration performance. The three figures are tested on the same chip and feature some fluctuation. The main result is that the measured power of the detected signal is not accurate, as the detected signal is close to the external ADC noise floor level. However, the measured results are enough for the system requirement of the SDR receiver.

VII. EXPERIMENTAL RESULTS

The SDR receiver has been implemented in 65nm CMOS. Fig. 20 shows the microphotograph of the chip, with the core area of about 5.4mm². The receiver draws 9.6-47.4mA from 1.2V power supply. For test purposes, the chip is directly bonded on PCB and configured through the SPI interface.

A. Small-Signal Performance

The measured conversion gain and NF are shown in Fig. 21. The measured optimized conversion gain and NF of the three

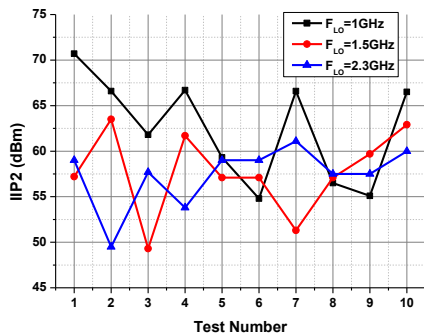


Fig. 17 Measured IIP2 of the main path for 10 tests

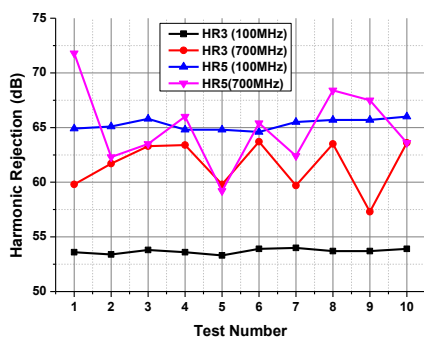


Fig. 18 Measured HR3/HR5 of the HR path for 10 tests

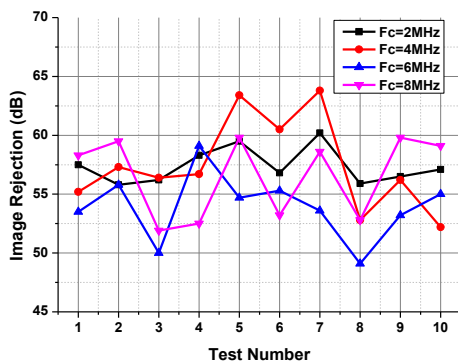


Fig. 19 Measured image rejection of the main path for 10 tests

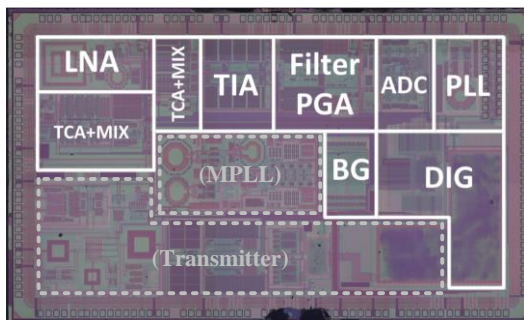


Fig. 20 Microphotograph of the SDR receiver

receiver paths is approximately 85dB and 3.8dB, and deteriorates at high frequency. The peaks and dips over the frequency range are due to the fact that the gains of various

LNAs vary when operating at different frequencies. It is shown that the NF of the sub path is worse than the main path. The reason is that the sub path is optimized to achieve high linearity, instead of low NF, since the sub path is mainly used in the strong interference scenario where the sensitivity requirement could be relaxed.

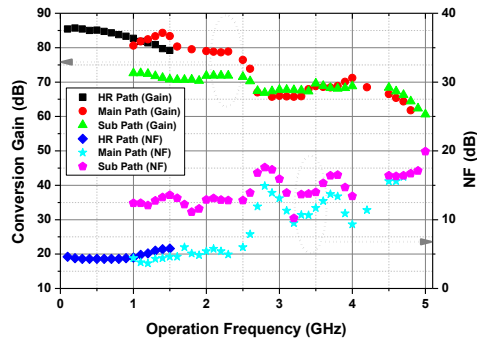


Fig. 21 Measured conversion gain and NF of main path, sub path and HR path receiver versus LO frequency

As three RF front-end paths reuse the TIA and LP/CBP baseband filter, they feature the similar transfer function. Several transfer function settings of the main path receiver front-end are shown in Fig. 22. The bandwidth of the 5th-order LP Butterworth filtering with 0dB conversion gain ranges from 0.7 MHz to 10 MHz. For the low-IF architecture, the center frequency of the CBP filter can be tunable from 2 MHz to 8 MHz, with a signal bandwidth of 2MHz.

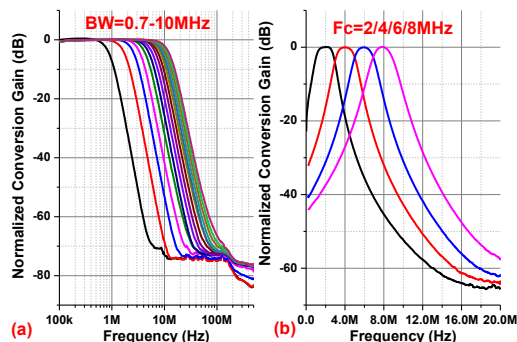


Fig. 22 Measured RX conversion gain with different LPF and CBP bandwidth of the main path receiver front-end

B. In-Band IIP3 and Out-of-Band IIP3/IIP2

Fig. 23 shows the measured in-band (IB) and out-of-band (OB) IIP3 of the main path, sub path and HR path receiver front-ends versus LO frequency, where the receiver BW is set to 20MHz. For IB-IIP3 test, two tones ($f_1=f_{LO}+5$ MHz, $f_2=f_{LO}+5.1$ MHz) as well as the 3rd-order intermodulation product are all the in-band signals. The measured IB-IIP3 of the main path, sub path and HR path are around +5dBm, +10dBm and +13dBm, respectively, thanks to the high linear LNAs. For OB-IIP3 test, two tones ($f_1=f_{LO}+200$ MHz, $f_2=f_{LO}+395$ MHz) are far away from the LO frequency. The measured OB-IIP3 of the main path, sub path and HR path are around +5dBm, +18dBm and +14dBm, respectively. Thanks to the RF filtering, the OB-IIP3 is significantly improved compared with the IB-IIP3 of the sub path.

For OB-IIP2 test, two tones ($f_1=f_{LO}+100$ MHz, $f_2=f_{LO}+105$ MHz) are far away from the LO frequency. Fig. 24 shows the OB-IIP2 of the sub path receiver front-end versus digital calibration code, indicating that the OB-IIP2 in excess of +65dBm can be achieved through calibration. Fig. 24 also shows the measured OB-IIP2 of the main path and sub path receiver front-end with maximum bandwidth versus LO frequency. From 1 GHz to 5 GHz, the measured auto calibration OB-IIP2 of the main path and sub path are around +61dBm and +62dBm, respectively. The OB-IIP2 of the main path is similar to the OB-IIP2 of the sub path since the second-order intermodulation of the receiver is mainly caused by the mismatch in the mixer, and the main path is configured into low gain mode in the two tone test.

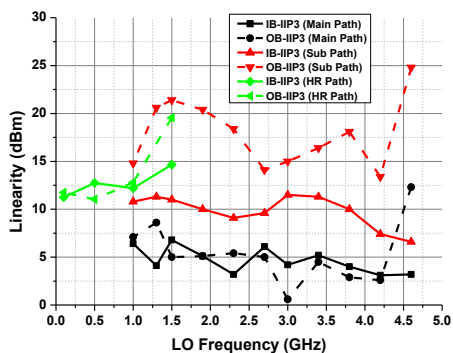


Fig. 23 Measured IB/OB-IIP3 of the main path, sub path and HR path receiver front-end versus LO frequency

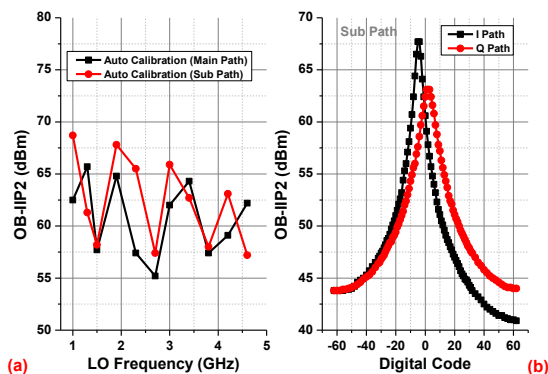


Fig. 24 Measured OB-IIP2 versus calibration code of the sub path, and OB-IIP2 of the main path and sub path receiver front-end

C. 3rd-order and 5th-order Harmonic Rejection

To test the performance of the harmonic rejection, testing tones at $3*f_{LO}+5$ MHz are applied to the input of the receiver front-ends for the HR3 test, and testing tones at $5*f_{LO}+5$ MHz are applied for the HR5 test. Fig. 25 shows the measured HR3 and HR5 of the main path (1.0 GHz-3.0 GHz) and HR path (100 MHz-1.5 GHz), with and without auto calibration. For the low frequency band HR path, an improvement of about 30-40dB rejection is achieved with auto calibration. Compare with [27], the auto calibration achieves similar HR improvement with the manual calibration. For the high frequency band HR path, auto calibration is limited by the noise floor of the ADC. Besides, with the help of the off-chip inductor formed passive LPF, the HR3 and HR5 improve as LO frequency increases. For the

main path, the HR3/HR5 is higher than 40dB/50dB due to out-of-band rejection of the tunable LC tank of LNA. For above 3.0 GHz frequency band, harmonic rejection is not deemed necessary.

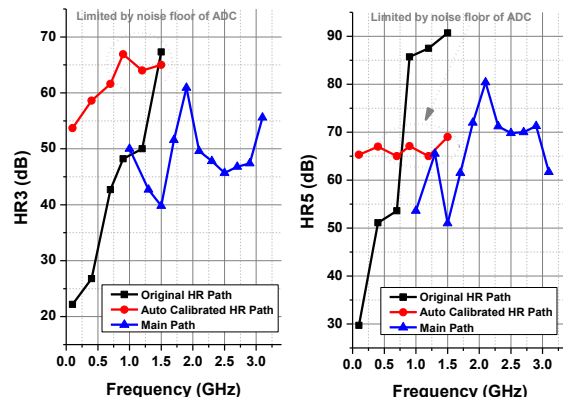


Fig. 25 Measured HR3 and HR5 versus LO frequency of the HR path (with/without calibration) and main path receiver front-end

D. Blocker Performance

Fig. 26 shows the measured RF filtering performance of the sub path receiver front-end. When the TIA and analog filter are set to maximum bandwidth, the RF filter offers about 10dB rejection at 10 MHz offset. Blocker performance has been measured by means of blocker compression and blocker noise figure, as shown in Fig. 27. The test tone is located at $f_{RF}=1$ GHz for the HR path and $f_{RF}=1.5$ GHz for the main path and sub path, and the blocker is located at $f_{blocker}=f_{RF}+100$ MHz, i.e. 1.1GHz for the HR path and 1.6GHz for the main and sub path. The conversion gain is compressed by 1dB in the presence of a -22dBm blocker for the HR path and -27dBm for the main path, while the conversion gain of the sub path is compressed by 1dB in the presence of a -6dBm blocker, thanks to the RF filtering.

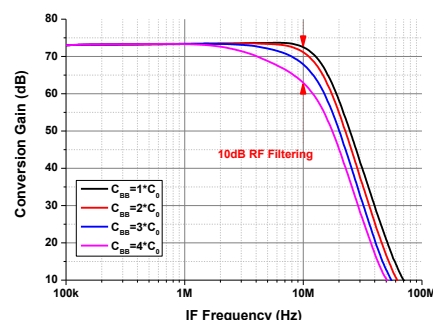


Fig. 26 Measured RF filtering of the sub path receiver front-end

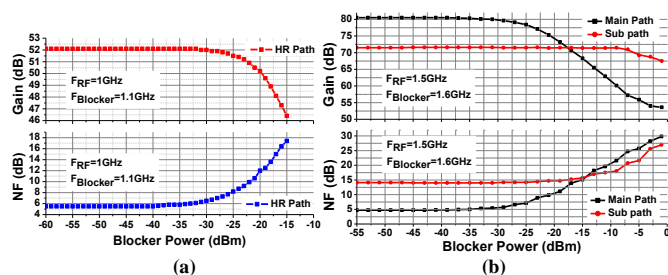


Fig. 27 Measured blocker compression performance and NF, (a) the HR path receiver front-end, (b) the main path and sub path receiver front-end

E. CTΣ-Δ ADC

The ADC is measured separately, and the FOM varies from 0.18 to 0.49 pJ/conv. over various modes. Fig. 28 shows the measured SNDR performance of the main path receiver front-end versus input power with on-chip ADC and off-chip ADC (AD9648: 14-Bit, 125MSPS). The tone test is processed including noise and six harmonics (the 2nd-order to 7th-order harmonics) below half of sampling frequency. Either using an off-chip or on-chip sampling clock, there is no significant difference. Compared with the receiver front-end with the off-chip ADC, SNDR of the whole receiver (including the cascaded integrator-comb (CIC) and finite impulse response (FIR) filter) with the on-chip ADC shows 6-9dB improvement, as the CIC and FIR filter can filter out the out-of-band noise and harmonics.

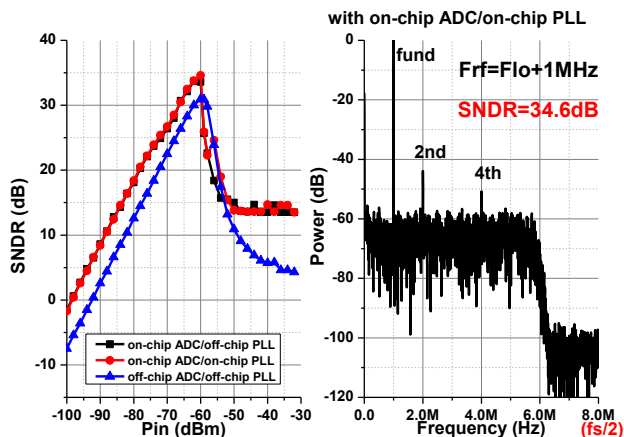


Fig. 28 Measured SNDR performance versus input power with on/off-chip ADC and PLL of the main path receiver front-end

F. Image Rejection Ratio

Fig. 29 shows the measured image rejection ratio for 2-8

MHz center frequency with 2 MHz bandwidth. After the auto calibration, the average image rejection ratio over 10 tests is around 55dB, with about 12dB improvement from the calibration.

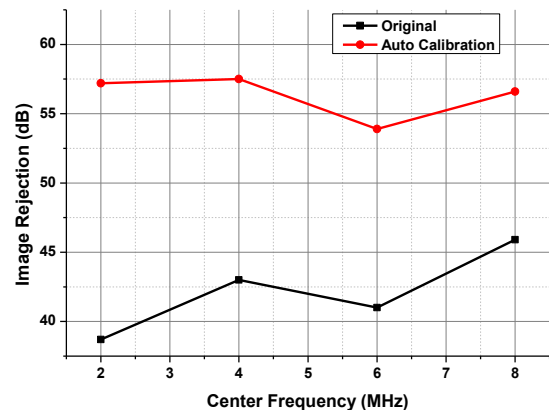


Fig. 29 Measured image rejection with I/Q calibration

G. System Performance: SNDR and EVM

Fig. 30 shows the measured SNDR and EVM of the main/HR path receiver front-end as a function of the input power for multiple carrier frequencies and bandwidths. The receiver gains are set according to noise and interference. SNDR measurements are performed with off-chip ADC, with noise and six harmonics (the 2nd-order to 7th-order harmonics) below half the sampling frequency being all counted, and EVM measurements use 32QAM modulation. The HR path achieves 2.3% EVM, better than the main path. The main reason is that the HR path works in lower frequency and narrower bandwidth mode in the EVM test.

TABLE III SDR RECEIVER PERFORMANCE SUMMARY

Mode	600MHz_8MHz (HB Path)	1.8GHz_20MHz (Main Path)	2.4GHz_20MHz (Main Path)	2.4GHz_2MHz (Main Path)	3.3GHz_20MHz (Main Path)	4.3GHz_20MHz (Main Path)
RX	Zero-IF	Zero-IF	Zero-IF	Low-IF	Zero-IF	Zero-IF
Fc (GHz)	0.6	1.8	2.4	2.4	3.3	4.3
Signal BW (MHz)	8	20	20	2	20	20
Max Gain (dB)	84	74	79	79	73	72
Main Path: IB/OB_IIP3 (dBm)	-	5.1/5.1	3.2/5.4	3.5/5.5	5.2/4.5	3.1/2.6
Sub Path: IB/OB_IIP3 (dBm)	-	10/20.4	9.1/18.4	9.5/18.7	11.3/16.4	7.4/13.4
HR Path: IB/OB_IIP3 (dBm)	12.8/11.1	-	-	-	-	-
Main Path: IIP2 (dBm)	-	64.8	57.4	-	64.3	59.1
Sub Path: IIP2 (dBm)	-	67.8	65.5	-	62.7	63.1
IRR (dB)	-	-	-	55	-	-
HR3/HR5 (dB)	61.5/65	-	-	-	-	-
Power (mA)*	15.1-24.7	25-42.7	25.9-43.6	18-33.1	27.3-45	29-46.8
Modulation	32QAM	32QAM	32QAM	-	32QAM	32QAM
EVM (%)	2.3	5.1	5.4	-	5.1	5.3
Sensitivity test (with an external LO)						
Mode	600MHz_8MHz (HB Path)	1.8GHz_20MHz (Main Path)	2.4GHz_20MHz (Main Path)	2.4GHz_2MHz (Main Path)	3.3GHz_20MHz (Main Path)	4.3GHz_20MHz (Main Path)
Pin (dBm)	-84	-93	-65	-85	-75	-67
SNDR (dB)**	17.4	2.4	29.7	17	12.6	21
Reference Standard required SNDR	DVB-H (16QAM) 13.7	LTE (QPSK) 2	802.11g (64QAM) 27	ZigBee (O-QPSK) 1	-	LTE (64QAM) 18

* Does not include power of digital circuits; ** Tone test including noise and six harmonics below half of sampling frequency (fs=2.5*BW)

TABLE IV
COMPARISON WITH THE STATE-OF-THE-ART SDR RECEIVERS

	[2]	[6]	[10]	[29]	[30]	[31]	[32]	This Work
System	RX+FS	RX	RX+ADC	RX	RX	RX+FS	RX+FS	RX+ADC+Dig
Frequency (GHz)	0.4-6	0.4-0.9	0.4-6	1.8-2.4	0.08-2.7	0.1-5	0.5-3	0.1-5
Signal BW (MHz)	3-40	12	1-100	1.4/3.4	-	1-40	8	0.005-20 ^a
Max Gain (dB)	70	34	70	45.5	70	84	35	85
NF (dB)	3	3.5	1.8	3.8	1.5	2.8	6.8	3.8 (Main Path) 10 (Sub Path) 4.3 (HR Path)
IB-IIP3 (dBm)	+6	+3.5	-	-	-	-4	-12.4	+5 (Main Path) +10 (Sub Path) +13 (HR Path)
OB-IIP3 (dBm)	+10	+16	+5	+18	+13.5	-	+11.7	+5 (Main Path) +18 (Sub Path) +14 (HR Path)
IIP2 (dBm)	+70	+56	>+85	+64	-	+36	+58	+61 (Main Path) +62 (Sub Path)
IRR (dB)	-	-	-	-	-	-	-	56
HR3/HR5 (dB)	-	60/64	>70/50	54/65	42/45	-	47/52	62/66 (HR Path)
Auto Calibration	No	Yes	No	No	No	No	No	Yes
Power (mW)	64-100	60	40	32	15.6	59.4-115.5	250-600	11.5-56.9 ^b
Voltage (V)	1.2/2.5	1.2	0.9	1.2/1.8	1.3	1.1	1.2	1.2
Technology	40nm	65nm	28nm	40nm	40nm	45nm	65nm	65nm

a 5kHz bandwidth is provided by CIC and FIR; b Does not include power of digital circuits

H. Performance Summary

TABLE III summarizes the performance across six selected standard configurations. In the sensitivity characterization, P_{in} at each frequency is set to the value defined by the reference standard. The sensitivity of the SDR receiver satisfies the requirements of all listed wireless communication standards. The measurement results of the proposed SDR receiver are compared to other state-of-the-art receivers in TABLE IV. The proposed SDR receiver achieves high integration level, wide bandwidth coverage, high IB/OB-IIP3 and IIP2, and low power consumption.

with out-of-band blocker rejection based on voltage-mode passive mixer, and a HR-path with vector harmonic rejection calibration. Dual-feedback LNA with “8”-shaped nested inductor are proposed, cascading with Miller feedback compensated TCA. Power-scalable class-AB Op-Amp is presented with Miller feed-forward compensation and QFG technique to improve the GBW and reduce power consumption. Digitally assisted calibrations for HR, IIP2 and IR are presented to maintain high performances over PVT variations.

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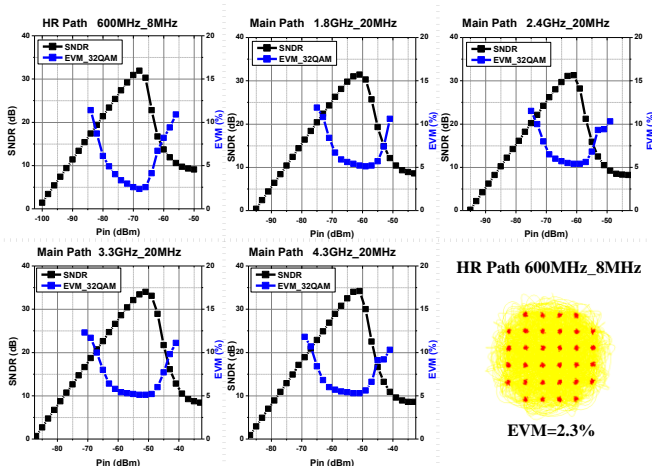


Fig. 30 Measured SNDR and EVM versus input power for multiple carrier frequencies and bandwidths of the main/HR path receiver front-end, EVM of HR path 600MHz_8MHz

VIII. CONCLUSION

A 0.1-5.0 GHz flexible SDR receiver with digitally assisted calibration is presented. It supports both wideband and narrow bandwidth applications with zero-IF/low-IF reconfigurable architecture. To achieve high robustness against out-of-band blockers and harmonic interferences, the receiver employs three paths in the RF front-end, including a low noise main-path based on current-mode passive mixer, a high linearity sub-path

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