A Neural Network Approach For Fault Diagnosis Of Large-scale Analogue Circuits

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Abstract: An approach for fault diagnosis of large-scale analogue circuits using neural networks is presented in the paper. This method is based on the fault dictionary technique, but it can deal with soft faults due to robustness of neural networks. Because the neural networks can create the fault dictionary, memorize and verify it simultaneously, computation time is drastically reduced. Rather than dealing with the whole circuit directly, the proposed approach partitions a large-scale circuit into several small sub-circuits and then tests each sub-circuit using the neural network method. The principle and diagnosis procedure of the method are described. Two examples are given to illustrate the method for both small and large-scale circuits.

1. Introduction

Fault detection and diagnosis (FDD) has become an active research area since 1970's and the past decade has seen some promising progress in the field of analogue FDD [1-9]. Various useful techniques have been suggested in the literature, which include the fault dictionary technique, parameter identification technique, optimization-based technique and neural network (NN) technique. These techniques can be normally divided into two general categories [2]: the estimation methods and pattern recognition (PR) methods. Estimation methods require mathematical process models that represent the real process satisfactorily. These models should not be too complicated, otherwise computation will become very time-consuming. This limits the application of these methods. In pattern recognition methods for FDD, however, no mathematical model of the process is necessarily needed. The idea behind these methods is that the operation of the process is classified according to measurement data. Formally, this is a mapping from measurement space into decision space. Traditional pattern recognition and classification can be divided into three stages: measurement, feature extraction and classification. PR methods are usually computationally easier but the calculation task depends very much on the data and the actual problems.

Although much progress has been made, analogue circuit FDD remains extremely difficult and becomes the bottleneck of automatic testing of mixed-signal circuits. This is because of the difficulty of measuring currents, the lack of good fault models similar to the stuck-at-one and stuck-at-zero fault models in digital circuit test, the tolerance of components and the nonlinear nature of analogue circuits (the relationship between the circuit responses and the component characteristics is nonlinear, even if the circuit is linear). Therefore, only the fault dictionary technique is widely appreciated in practical engineering applications among the various techniques in the literature because of its simplicity and the effectiveness. However, it has its own vital weakness, that is, it can only detect hard faults and cannot cope with soft faults. Also, its application is largely limited to small to medium analogue circuits.

A neural network based fault diagnosis method for large-scale analogue circuits is proposed in the paper. The method can detect both hard and soft faults because the BPNNs are capable of robust classification even in the noisy environments. The process of creating the fault dictionary, memorizing the dictionary and verifying it are simultaneously completed by the BPNNs, thus the computation time is drastically reduced. This makes it possible to diagnose faults on line.

2. Neural Networks

Neural networks (NN) have been applied to a variety of problems in the areas of pattern recognition, signal processing, image processing, process identification, etc. Some researchers have successfully applied NNs to fault diagnosis of chemical processes, automotive engine failure, and even digital circuitry. But not much work has been done to use NNs for fault diagnosis of analogue circuits [3], especially large-scale analogue circuits.

The most popular NN architecture is the backward error propagation (BP) network. It is a supervised network that has shown promise in pattern classification. Typical BP networks have two or three layers of interconnecting

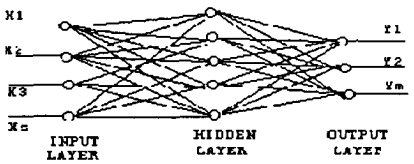

Fig. 1 BP network

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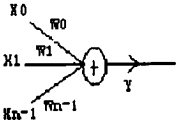
weights. Fig.1 shows a standard two layer network. It is a fully connected topology because each input node is connected to a hidden layer node, and each hidden node is connected to an output node in a similar fashion. The neuron's structure is shown in Fig.2, where xi (i=0,1,2...n)



$$Y = f(\sum_{i=0}^{n-1} W_i X_i - \theta_i)$$

Fig. 2. Neuron of BPNN

are the inputs, w_i (i=0,1,2...n) are the weight coefficients, θ is the characteristic offset (bias), f(x) is the transfer function and Y is the output. In general, practical applications require an NN being non-decreasing and differentiable at all times. However, f(x) may be linear or non-linear. A common function is a sigmoid function: f(x) =1/[1+exp(-x)]

Learning takes place by propagating the node activation of output patterns to the output node. The BPNN can be trained to provide signal estimation and pattern recognition if appropriate input and output pairs are given. And a detailed description of the BP algorithm can be found in the abundant literature.

3. Diagnosis Principle Using BPNN

A large-scale analogue circuit can be torn into several sub-circuits according to some certain rules, for example, according to its structure or function. Each sub-circuit matches a certain BPNN, as shown in Fig.3.

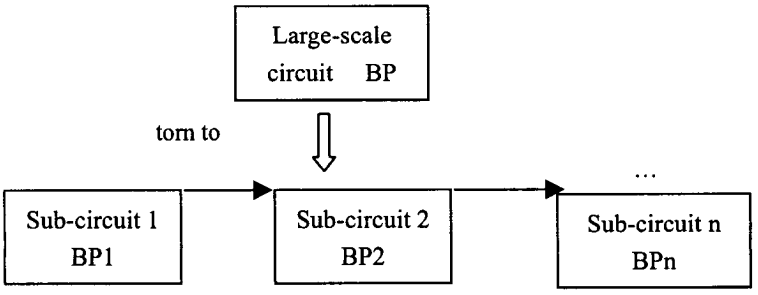


Fig. 3. Basic diagnosis principle

3.1. Diagnosis Principle of Sub-circuits

For the construction of the fault dictionary, the circuit under test (CUT) is simulated using PSPICE software. Firstly, a signal is applied to the input of the CUT with nominal component values and accessible node voltages are obtained for the fault-free circuit. We call the ith-node voltage U_{io}. Applying the same stimulus to the circuit, the accessible node voltages are obtained from the files created by PSPICE for each chosen fault in the set of possible faults. The ith accessible node voltage of the faulty circuit is denoted as U_i. The difference of the accessible node voltage due to the fault is $\Delta U_i=U_i-U_{i0}$.

In a linear circuit, suppose that x is the single fault branch (component), then the expression $\Delta U_i / (\sum_{j=1}^{m} \Delta U_j^2)^{1/2}$ (i=1,2 ... m, m is the number of accessible nodes) is a constant no matter whether the fault is a soft one or a hard one, and it depends only on the topology and its normal parameter values. So $\Delta U_i / (\sum_{j=1}^{m} \Delta U_j^2)^{1/2}$ can be extracted as the feature vector passing through the BPNN. The BPNN will not be trained ready until it converges onto the target value. The above process must be done before test. After test, the measured feature vector is applied to the trained BPNN, and the output of the BPNN is the number of the faulty branch/component. The steps involved in the fault diagnosis of a sub-circuit can be summarized as:

1). define faults of interest
2). apply the test signal to the CUT and calculate the feature vectors under various faulty or fault-free conditions
3). pass the feature vectors through the BPNN and train the BPNN
4). identify the fault class at the output of the BPNN
5). measure and calculate the practical feature vector and apply it through the trained BPNN

3.2 Diagnosis Method of Large-scale Circuits

A large-scale circuit may be torn into a number of sub-circuits. Each sub-circuit can be diagnosed using an independent BPNN as discussed Section 3.1. Thus the diagnosis procedure for a large-scale circuit can be easily summarized as:

① Divide the large-scale circuit into sub-circuit 1, sub-circuit 2, ..., sub-circuit n

②. Define the faults of interest for each sub-circuit
③. Apply an appropriate signal to the large-scale circuit, measure accessible node voltages, and calculate feature vectors
④. For each sub-circuit, pass the feature vectors through the corresponding BPNN under the fault-free and different faulty conditions and train the BPNN
⑤. Calculate the measured feature vector of sub-circuit 1 and apply it through the trained BP1,
⑥. Identify the fault class at the output of BP1;
⑦. Repeat steps 5 and 6 for sub-circuits 2, 3,..., until the last sub-circuit n.

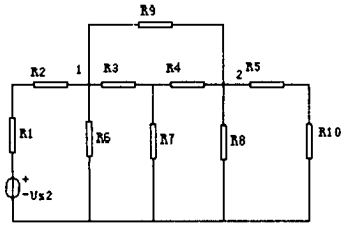


Fig. 4 simulated example 1

4. Examples

Consider the circuit shown in Fig. 4. The marked parameters are: $R_1=R_{10}=10\ \Omega$, $R_i=1k\ \Omega$ (i=2, 3,...8), $R_9=500\ \Omega$, and $U_{S1}=5V$. Suppose that nodes 1 and 2 are accessible. This is a small circuit and so we deal with it directly. According to Section 3.1, the diagnosis process can be conducted using the following steps:

1). The feature vectors were computed under the fault conditions shown in Table 1.

2). These feature vectors were passed through a neural network repeatedly. The neural network was a three-layer BP network, which has 2 inputs, 8 hidden layer 1, 8 hidden layer 2, and 3 outputs. The fault dictionary was created after the network was trained.

3). When the circuit is faulty, the trained BP is needed to diagnose the faults. The outputs (U1, U2) were measured and the feature vector was calculated. The feature vector was then passed through the BP network. The fault element was identified by the output of the BP.

A second circuit is shown in Fig.5. This is a large-scale circuit. It is decomposed into 4 sub-circuits (marked in red lines), denoted by x_1, x_2, x_3, x_4, according to the nature of the circuit. Assume that R_{14} and Q_3 are faulty, and the value of R_{14} is changed to 450ohm, the base of Q_7 is open. Following the steps in Section 3.2, Table 2 was produced, containing accessible node voltages.

The feature vectors were passed through the corresponding BPNNs, and the following results were obtained from the outputs of the BPNNs: sub-circuit 1 (x_1) and sub-circuit 4 (x_4) were fault-free, sub-circuit 2 (x_2) and sub-circuit 3 (x_3) were faulty. The faulty elements were identified as Q_3 and R_{14}, which are the same as originally assumed.

5. Conclusions

A neural network based method for fault diagnosis of large-scale analogue circuits has been proposed in the paper. This approach is robust because the BPNN is capable of robust classification even in the noisy environments. On-line computation time is reduced from the traditional techniques, although the simulation amount before test is still large. A major advantage of the BPNN method shown is the capability of diagnosing soft faults a difficult problem for the traditional dictionary technique. Further work is going on to use the proposed method to diagnose complex fault combinations in very large-scale analogue circuits.

Acknowledgment

This work is supported by the Natural Science Youth Funding Council of China under Grant No.59707002, and Chinese Education Ministry's Aid Plan of Backbone Teachers of Colleges and Universities by (No.[2000] 65).

Fault elements			R_4				R_7	
Fault types		Fault-free	R_4 SC	R_4 OC	R_4=200	R_4=50	R_7 SC	R_7 OC
U_1		1.4194	1.4167	1.4194	1.4194	1.4194	1.1819	1.5979
U_2		0.7112	0.7064	1.7115	1.7110	1.7109	0.4737	0.8897
Feature vector	Element1	0	0.4481	0.4481	0.4479	0.4480	0.4969	0.4945
	Element1	0	0.8940	0.8940	0.8941	0.8941	0.8678	0.8789

Fault element		R_7		R_3			
Fault type		R_7=200	R_7=50	R_3SC	R_3OC	R_3=200	R_3=50
U_1		1.2694	1.2079	1.1825	1.5973	1.2698	1.2084
U_2		0.512	0.4997	0.7109	0.7115	0.7110	0.7109
Feature vector	Element1	0.4811	0.4924	0.5554	0.5518	0.5181	0.5448
	Element1	0.8767	0.8704	0.8316	0.8361	0.8551	0.8386

Table1. Part of the data of the fault dictionary (SC-:short circuit, OC-:open circuit)

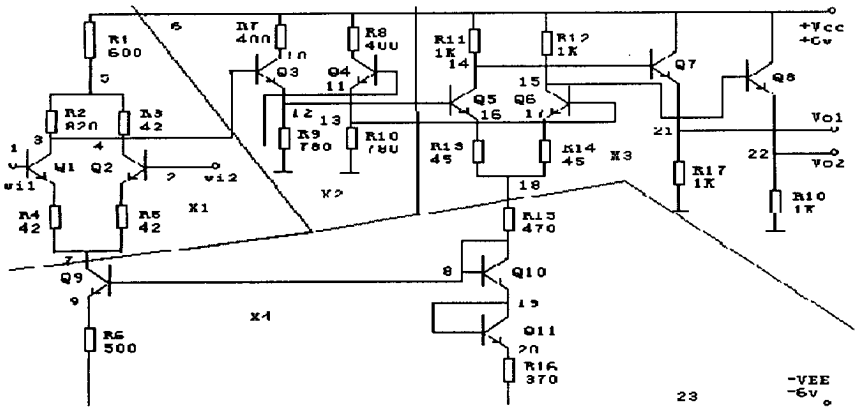


Fig.5. Simulated example 2: a large-scale circuit

NN	Items	Values					Feature vectors
BP 1	Node order no.	3	4	6	7		0 0 0 1
	Node voltage V_{io}	1.0122	1.0122	6.0000	-0.8422		
	Node voltage V_i	1.3384	1.3152	6.0000	-0.8330		
BP 2	Node order no.	7	12	13			0.0223 0.8171 0.5760
	Node voltage V_{io}	-0.8422	0.3233	0.3233			
	Node voltage V_i	-0.8330	-0.0146	0.5615			
BP 3	Node order no.	8	14	15	21	22	.0213 .1040 .4978 .7829 .3578
	Node voltage V_{io}	-2.7457	3.6267	3.6267	2.8859	2.8859	
	Node voltage V_i	-2.9178	2.7878	-.3886	2.0556	7.275e-9	
BP 4	Node order no.	7	8	23			.0535 .9986 0
	Node voltage V_{io}	-0.8422	-2.7457	-6.0000			
	Node voltage V_i	-0.8330	-2.9178	-6.0000			

Table 2 Diagnosis data for example 2 (V_{io} are the nominal accessible node voltages and V_i the measured)

References

[1] R. Spain and S. Upadhyaya, "Linear circuit fault diagnosis using neuromorphic analyzers", IEEE Trans. CAS-II. Vol.44, No.3, pp.188-196, 1997.

[2] T. Sorsa, H. N. Koivo, and H. Koivisto, "Neural networks in process fault diagnosis", IEEE Trans. on Systems, Man and Cybernetics, Vol.21, No.4, 1991.

[3] A. Bernieri, M.D'Apuzzo, L.Somsone, etc, "A neural network approach for identification and fault diagnosis of dynamic systems", IEEE Trans. IM, Vol.43, No.6, 1994.

[4] A. Srinivasan and C. Batur, "Hopfield/Art-1 neural network-based fault detection and fault diagnosis of dynamic systems", IEEE Trans. on Neural Networks, Vol.5, No.6, 1994.

[5] Y. He and Y. Sun, "Neural networks-based L1-norm optimization approach for fault diagnosis of nonlinear circuits with tolerance," IEE Proceedings: CDS, Vol. 148, No.4, 2001.

[6] Y. He and Y. Sun, "Fault isolation in nonlinear analog circuits with tolerances using neural networks," Proc. IEEE Int. Symp. Circuits and Systems, Sydney, 2001.

[7] Y. Sun, "Cut-fault diagnosis of nonlinear circuits," Proc. Int. Conf. on Circuits and Systems, Nanjing, China, 1989.

[8] Y. Sun and J. K. Fidler, "A topological method of class-fault diagnosis," Proc. IEEE Midwest Symp. on CAS, USA,1992.

[9] H.-T. Sheu and Y.-H. Chang, "Robust fault diagnosis for large-scale analog circuits with measurement noises", IEEE Trans. CAS-I, Vol. 44, pp:198-209, 1997.