A low-power, high-linearity transconductor with high tolerance for process and temperature variations

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Abstract: A novel scheme for tunable CMOS transconductor robust against process and temperature variations is presented. The proposed configuration is a voltage controlled circuit based on a double NMOS transistor differential pairs connected in parallel, which has low power and high linearity. The process and temperature (PT) compensation is completed by two identical process and temperature compensation bias voltage generators (PTCBVG), which can guarantee the designed transconductor high tolerance for process and temperature variations. A complete CMOS transconductor with PTCBVG has been designed and simulated using 0.18μm technology. The effectiveness of PT compensation technique is proved. The simulation results of post-layout are commensurate with pre-layout. Post-layout simulation results show that when temperature changes from −40-85°C for different process corners (TT, SS, SF, FS, FF), the transconductance varies from 91.8-123.6μS, temperature coefficient is below 1090ppm/°C, the total harmonic distortion is from −78-−72dB@1MHz for 0.2V_{PP} input signal, -3dB bandwidth changes from 2.5-5GHz, input referred noise varies from 78.1-124.8nV/sqartHz@1MHz and DC power is from 1.5-3.2mW.

1. Introduction

The CMOS transconductor is a fundamental building block for analog signal processing circuits, such as amplifiers, multipliers, active filters and sinusoidal oscillators. Throughout the development of the state of the art, we can conclude that the performance indices of most concern about transconductor include high linearity, process and temperature (PT) compensation ability and low power.

The first and most important performance of the CMOS transconductor is its linearity. Up to now, all kinds of topologies of the CMOS transconductor have been presented for improving the linearity property. The main structure of the transconductor cell is the source-coupled differential pair, which has good CMRR, PSRR, low noise and excellent frequency performance. However, its large signal characteristics are nonlinear. Many advances in improving the linearity of CMOS transconductor circuits have been reported [1-25]. In [1], it proposes a tranconductor with compensated source-coupled pair configuration. The circuit discussed have superior linearity and input voltage range compared with the conventional source-coupled differential pair. The proposed tranconductor has a THD of approximately 0.1% covering one half the input voltage range, whereas the source-coupled pair exhibits a maximum error greater than 10% within this range. However, the bandwidth of the presented transconductor is only up to 6MHz by the simulation which is unsuitable for high frequency applications. In [2], it uses an approach to linearization by an electronically controlled current-mode cell. The linearity and input voltage range of the proposed circuits are significantly improved over those of the conventional source-coupled differential pair. The SPICE Simulated results show a linearity error less than 0.2% over ±4V differential input range for a power supply of ±5V. [5] presents a linear CMOS transconductor using triode transistors based on the scheme of flipped voltage follower current sensor. The transconductor cell biased in triode region presents simplicity and good programmability compared with its saturated-based counterpart. The proposed transconductor achieves a distortion of −72dB for a 1MHz, 1V_{PP} differential input voltage. [12-17] use the local feedback method to improve the linearity of the CMOS transconductor. The transconductor proposed by [12] is based in the creation of low impedance nodes using local feedback to drive a degeneration resistor. The presented transconductor doesn't use current mirrors or nonlinear cancellation method, which significantly improves the linearity and the robustness against mismatch. Simulation results show that the THD of the proposed transconductor can achieve −91dB at 10MHz with 2V_{PP} differential input-output signal. In [18-20], the source degeneration method is employed. [18] presents a programmable source degenerated telescopic cascade OTA improved by a very linear programmable degeneration resistor implemented with four quasi-floating-gates (QFS) transistors. The use of QFG transistors to implement the degenerated resistor has the advantage of providing programmability. What's more, the harmonic distortion factor for the resistor used here is better than the case of using a triode transistor as a resistance. The simulation results obtained show a THD of −61dB at 10MHz for a 1V_{PP} output voltage. [21-25] discuss the non-linearity cancellation method. Transconductors with differential pairs based on nonlinearity cancellation have demonstrated good performances at high frequencies, but the process and temperature variations will greatly reduce the effectiveness of nonlinearity cancellation method. [22] presents a nonlinearity cancellation technique low sensitive to process-temperature-bias current variations. The proposed OTA is realized by using complementary triple differential pairs. Experimental results of the proposed circuit show that the transconductor achieves IM3=−70dB for a two-tone 1.3V_{PP} input signal for frequencies up to 70MHz with 9.5mW of power consumption.

Recently, for broadening the application of the CMOS transconductor, how to improve the tolerance for process and temperature variations has received more and more attention. [29] presents a fully on-chip process and temperature (PT)-invariant transconductor circuit that doesn't need any accurate quantity or trimming/calibration. The proposed transconductor employs a PTAT voltage generator, a process tracking circuit and a beta multiplier-based bias circuit. Measurement results show that the transconductance varies only by ±3.4% across 18 fabricated chips and over temperatures ranging from 25°C to 100°C. [32] presents a tunable body biasing voltage generated by auxiliary bandgap, LDO and body voltage control circuit to calibrate the transconductance induced by temperature. The accuracy of the tansconductor is nearly ±0.092%. However, the simulation results of [32] can't support its conclusion, because the influence of process variations and device mismatch on the transconductance variation is competitive to the temperature variation. More simulation work especially the montecarlo simulations need to be performed to verify the effectiveness of the theoretical analysis in [32].

Also, there are many reports about the low power design of the CMOS transconductor. The most popular low power topology of the transconductor is the pseudo differential pair [13, 26-27]. However, the pseudo differential structure usually has poor rejection to common-mode signals, which therefore can originate a large amount of distortion. The common-mode feedback circuit can overcome this drawback, but it increases both noise and power consumption. Although the technique for common-mode signals cancellation has been used, the CMRR performance of the pseudo-differential transconductor is inferior to the classical fully-differential one particularly at low frequency [26].

According to the discussion above, this paper employs a double differential pairs as the topology of the CMOS transconductor and the process and temperature compensation bias voltage generator (PTCBVG) to complete the process and temperature compensation function of the transconductor. The basic principle of the circuit is described in section II. The design scheme for process and temperature compensation is discussed in section III. Simulation results are presented in section IV. Conclusions are drawn in section V.

2. The basic principle of the transconductor

Fig. 1 provides the basic circuit diagram of the proposed CMOS transconductor core, V_{inP} and V_{inN} are the two differential input voltages, and I_{oP} and I_{oN} are the two differential output currents. The topology of the proposed transconductor in Fig. 1 is based on a double NMOS transistor differential pairs connected in parallel, which is similar to the topology in [28]. As is shown in Fig. 1, the double NMOS transistor differential pairs consist of two NMOS transistor differential pairs of M_{N1T} and M_{N2T}, and M_{N3T} and M_{N4T}, which operate in their saturation regions. The current of I_1, I_2, I_3 and I_4 respectively represents the drain current of the NMOS transistor M_{N1T}, M_{N2T}, M_{N3T} and M_{N4T}. The drain current of PMOS transistor M_{P1T} equals I_1+I_3, and the drain current of PMOS transistor M_{P2T} equals I_2+I_4. The current mirrors of PMOS transistor M_{P1T}, M_{P3T} and M_{P5T}, PMOS transistor M_{P2T}, M_{P4T} and M_{P6T}, NMOS transistor M_{N14T} and M_{N17T}, and NMOS transistor M_{N13T} and MN_{18T} act as active loads, which make $I_{oP}=I_1+I_3-I_2-I_4$ and $I_{oN}=I_2+I_4-I_1-I_3$.

Now let us calculate the linearity property of the double differential pairs of the transconductor presented in Fig. 1. We assume that all the MOS transistors of the transconductor circuit work in saturation region. Without considering the second-order effects of the MOS transistors, the *I-V* characteristics of the proposed transconductor can be expressed as

$$I_1 = K_n \left(V_{inP} - V_A - V_{thn}\right)^2 \tag{1a}$$

$$I_2 = K_n \left(V_{inN} - V_A - V_{thn}\right)^2 \tag{1b}$$

$$I_3 = K_n \left[\left(V_{inP} - V_{T1}\right) - V_B - V_{thn}\right]^2 \tag{1c}$$

$$I_4 = K_n \left[\left(V_{inN} - V_{T1}\right) - V_B - V_{thn}\right]^2 \tag{1d}$$

$$I_{S1} = 2K_n \left(V_{T2} - V_{thn}\right)^2 \tag{1e}$$

$$I_{S2} = 2K_n \left(V_{T3} - V_{thn}\right)^2 \tag{1f}$$

where I_1, I_2, I_3 and I_4 are the drain currents of the NMOS transistor M_{N1T}, M_{N2T}, M_{N3T} and M_{N4T} respectively; I_{S1} and I_{S2} are the drain currents of the NMOS transistor M_{N5T} and M_{N6T}; V_{inP} and V_{inN} are the two differential input voltages; V_A and V_B are the terminal voltages of the node *A* and *B*; V_{T1}, V_{T2} and V_{T3} are the external DC voltages; V_{thn} is the threshold voltage of the NMOS transistor; $K_n=(1/2)\mu_n C_{ox}(W/L)$, where μ_n represents the electron mobility, C_{ox} is the gate oxide capacitance per unit area, and W and L are the width and length of the channel respectively. In (1a) to (1d), we assume that the double NMOS transistor differential pairs (M_{N1T}-M_{N4T}) have the same aspect ratio (W/L). For ease of analysis, as can be seen in (1e) and (1f) we also assume that the NMOS transistor M_{N5T} and M_{N6T} have twice the aspect ratio of the double NMOS transistor differential pairs.

We write the input voltages of the transconductor as

$$V_{inP} = V_1 + V_{id} \tag{2a}$$

$$V_{inN} = V_1 - V_{id} \tag{2b}$$

where V_1 represents the common-mode part of the input voltage and V_{id} is the differential-mode part of the input voltage.

Using KCL for node *A* and *B*, we can get

$$I_{S1} = I_1 + I_2 \tag{3a}$$

$$I_{S2} = I_3 + I_4 \tag{3b}$$

Substituting (1a)-(1f) and (2a)-(2b) in to (3a) and (3b), and calculating the difference between I_{S1} and I_{S2}, we can get

$$V_A = V_1 - V_{T2} \tag{4a}$$

$$V_B = V_1 - V_{T1} - V_{T3} \tag{4b}$$

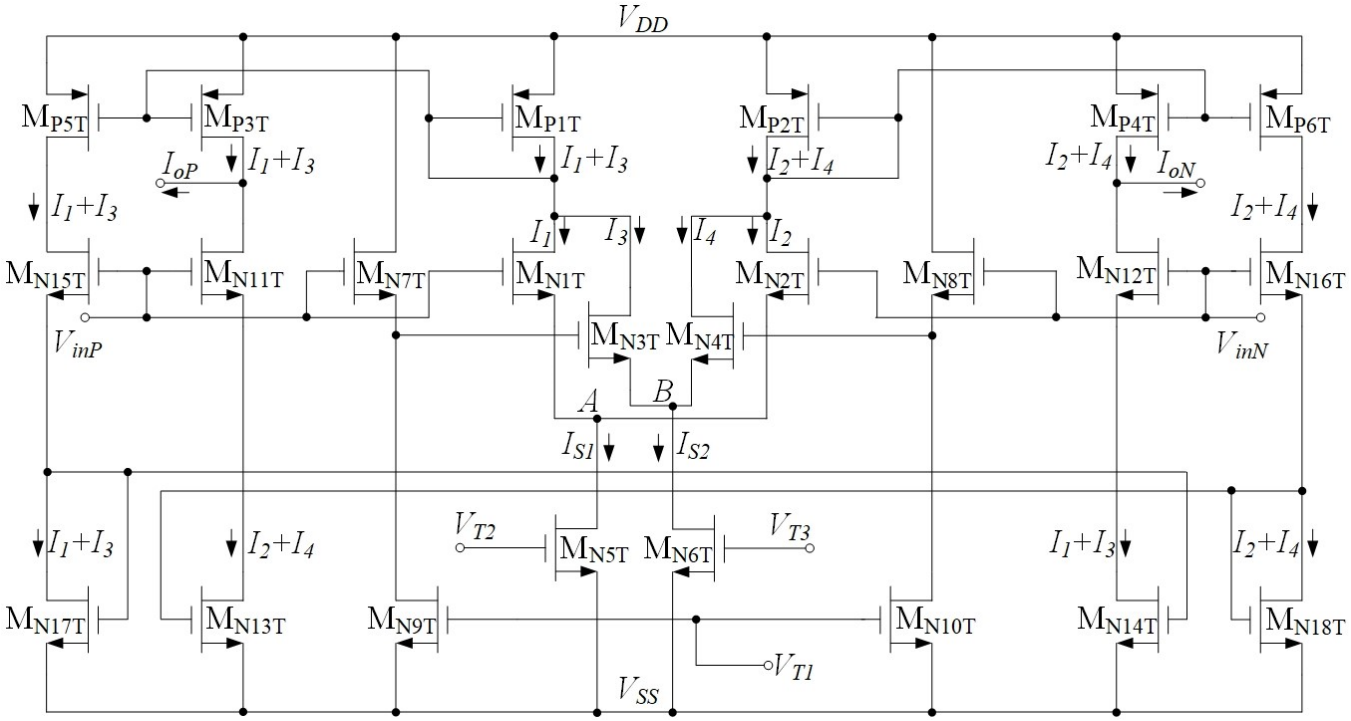

Fig. 1. *Basic circuit diagram of the proposed CMOS transconductor core*

Using (1a)-(1b), (2a)-(2b) and (4a), we can obtain the difference between I_1 and I_2

$$I_1 - I_2 = 4K_n V_{id}\left(V_{T2} - V_{thn}\right) \tag{5}$$

Using (1c)-(1d), (2a)-(2b) and (4b), we can also obtain the difference between I_3 and I_4

$$I_3 - I_4 = 4K_n V_{id}\left[V_{T3} - V_{thn}\right] \tag{6}$$

Now based on (5) and (6), the output currents of the transconductor become:

$$I_{oP} = I_1 + I_3 - I_2 - I_4 = 4K_n V_{id}\left(V_{T2} + V_{T3} - 2V_{thn}\right) \tag{7a}$$

$$I_{oN} = I_2 + I_4 - I_1 - I_3 = -4K_n V_{id}\left(V_{T2} + V_{T3} - 2V_{thn}\right) \tag{7b}$$

So the transconductance of the proposed transconductor can be expressed as

$$G_m = 4K_n\left(V_{T2} + V_{T3} - 2V_{thn}\right) \tag{8}$$

Observing (7) and (8), we can find that the linearity property of the double differential pairs of the proposed transconductor is expressed as an ideal linear mathematical model, and the transconductance is a constant which is proportional to the external DC voltages of V_{T2} and V_{T3}.

3. The design scheme for process and temperature compensation

According to [33], we can know that most process parameters vary with temperature, if a circuit is temperature-independent, then it is usually process-independent as well. So if the derivative of G_m in (8) with respect to the absolute temperature T, $\partial G_m/\partial T$, is equal to zero, the gain of the transconductor will be independent of both process and temperature. Based on this premise, we introduce a novel technique to complete the process and temperature compensation of the transconductor.

3.1. The design of process and temperature compensation bias voltage generator

The design scheme for process and temperature compensation of the proposed transconductor is illustrated in Fig. 2, which provides the circuit diagram of the devised process and temperature compensation bias voltage generator (PTCBVG). The presented PTCBVG is composed of a supply-independent biasing circuit, a PMOS core and an output part. All the MOS transistors of the PTCBVG work in saturation region except the PMOS transistors of M_{P4V}, M_{P5V} and M_{P6V} which are in subthreshold region. What's more, k is the aspect ratio of M_{P4V} and M_{P5V} to M_{P6V}, R_1 and R_2 are two voltage controlled resistors and V_T is the output voltage of the PTCBVG circuit.

First, we assume that the PMOS transistors of M_{P1V}, M_{P2V} and M_{P3V} have the same size, and so do the NMOS transistors of M_{N1V} and M_{N2V}. Next, tuning the DC bias point of the PTCBVG makes V_C=V_D. Then, we can acquire the same current flow behaviors of M_{P1V}, M_{P2V} and M_{P3V}: I_{sdP1V}=I_{sdP2V}=I_{sdP3V}=I_5, where I_{sdP1V}, I_{sdP2V} and I_{sdP3V} respectively represents the source-drain current of M_{P1V}, M_{P2V} and M_{P3V}.

In order to illustrate the working principle of the PTCBVG, we introduce a mathematical model of the source-drain current of the PMOS transistor (BSIM3V3 model) in subthreshold region, I_{sd}, given by [34]

$$I_{sd} = I_{s0}\left[1 - \exp\left(-\frac{V_{sd}}{nv_t}\right)\right]\exp\left(\frac{V_{sg} - V_{thp} - V_{OFF}}{nv_t}\right) \tag{9}$$

$$I_{s0} = \mu_p \frac{W_{eff}}{L_{eff}}\sqrt{\frac{q\varepsilon_{si}N_{CH}}{4\varphi_B}}v_t^2 \tag{10}$$

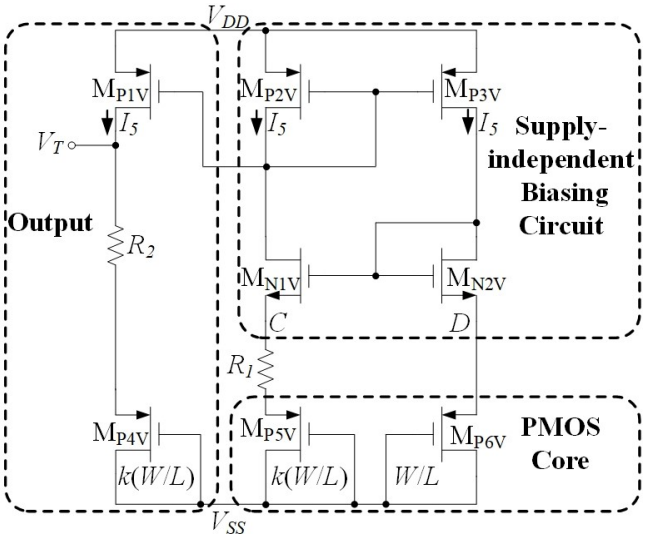

Fig. 2. *Basic circuit diagram of the proposed process and temperature compensation bias voltage generator*

where I_{s0} is a specific current; V_{sd} is the source-drain voltage of the PMOS transistor; n is the subthreshold swing factor, the typical value of which is 2; v_t is the thermal voltage, $v_t=K_BT/q$, where K_B is the Boltzmann constant and $K_B=1.4\cdot10^{-23}$J/K, T is the absolute temperature, and q is the electron charge; V_{sg} is the source-gate voltage of the PMOS transistor; V_{thp} is the threshold voltage of the PMOS transistor; V_{OFF} is an offset voltage of the BSIM3V3 model in the subthreshold region, the recommended range for which is between −0.06V and −0.12V. The default value of V_{OFF} is equal to −0.08V; μ_p is the mobility of holes; The effective channel length L_{eff} and channel width W_{eff} are used to characterize the MOSFETs in the compact model for circuit design; ε_{si} is the dielectric constant of the silicon; φ_B is a doping parameter relating the potential of an electron at the Fermi level to the doping concentration; N_{CH} is the channel doping concentration, the default value of which is $1.7\cdot10^{17}$(1/cm^3). As can be seen from (9), to ensure that I_{sd} exhibits an exponential dependence on V_{sg}, V_{sg} -V_{thp}-V_{OFF} must be less than 0.

If neglecting the influence of V_{sd}, (9) can be written as

$$V_{sg}-V_{thp}-V_{OFF}=V_{sgt}=nv_t ln\left(\frac{I_{sd}}{I_{s0}}\right) \tag{11}$$

where V_{sgt} represents the overdrive voltage of the PMOS transistor working in subthreshold region.

So the source-gate voltage difference of PMOS transistor M_{P6V} and M_{P5V}, V_{sgP6V}-V_{sgP5V}, can be expressed as

$$\begin{aligned} V_{sgP6V}-V_{sgP5V} &= nv_t\, ln\left(\frac{I_5}{I_{s0P6V}}\right)-nv_t\, ln\left(\frac{I_5}{I_{s0P5V}}\right) \\ &= nv_t\, ln\left(\frac{I_{s0P5V}}{I_{s0P6V}}\right) \end{aligned} \tag{12}$$

where I_5 is the source-drain current of the PMOS transistor M_{P5V} and M_{P6V}; I_{s0P5V} and I_{s0P6V} represent the specific currents of the PMOS transistor M_{P5V} and M_{P6V} respectively.

According to (10), (12) can be changed as

$$V_{sgP6V}-V_{sgP5V}=nv_t lnk \tag{13}$$

where k is the aspect ratio of M_{P5V} to M_{P6V}.

V_{sgP6V}-V_{sgP5V} also means the voltage drop across the resistor R_1, so the current flowing through R_1 is equal to nv_tlnk/R_1, which also equals the source-drain current of the PMOS transistor M_{P1V}, M_{P2V} and M_{P3V}. Then we can get the expression of V_T as

$$V_T=V_{sgP4V}-V_{OFF}+n\frac{R_2}{R_1}v_t lnk \tag{14}$$

where V_{sgP4V} is the source-gate voltage of the PMOS transistor M_{P4V}.

3.2. The complete schematic of the proposed transconductor

Fig. 3 shows the complete transconductor circuit, which contains three major parts: the CMOS transconductor core depicted in Fig. 1, and the two identical process and temperature compensation bias voltage generators (PTCBVG) depicted in Fig. 2 which are used to provide the external DC voltages of V_{T2} and V_{T3} for the CMOS transconductor core. Importantly, the resistor R_1 and R_2 in Fig. 2 are substituted by the NMOS transistor M_{R1} and M_{R2}, and M_{R3} and M_{R4} in Fig. 3, which are controlled by the DC voltage V_{R1}, V_{R2}, V_{R3} and V_{R4} respectively.

According to (14), we can get the expressions of V_{T2} and V_{T3}

$$V_{T2}=V_{sgP4V}-V_{OFF}+n\frac{R_2}{R_1}v_t lnk \tag{15a}$$

$$V_{T3}=V_{sgP10V}-V_{OFF}+n\frac{R_4}{R_3}v_t lnk \tag{15b}$$

where V_{sgP4V} and V_{sgP10V} represent the source-gate voltages of M_{P4V} and M_{P10V} respectively.

Assuming that $V_{thn}=V_{thp}$, then substituting (15a) and 15(b) into (8), we can get

$$G_m=4K_n\left(V_{sgtP4V}+V_{sgtP10V}+n\frac{R_2}{R_1}v_t lnk+n\frac{R_4}{R_3}v_t lnk\right) \tag{16}$$

The derivative of G_m in (16) with respect to the absolute temperature T can be expressed as

$$\frac{\partial G_m}{\partial T}=2C_{ox}\frac{W}{L}\frac{\partial\mu_n\left(V_{sgtP4V}+V_{sgtP10V}+n\frac{R_2}{R_1}v_t lnk+n\frac{R_4}{R_3}v_t lnk\right)}{\partial T} \tag{17}$$

By the way, μ_p in (10) and μ_n in (17) can be expressed as [35]

$$\mu_p=\mu_{op}\left(\frac{T_{NOM}}{T}\right)^{|\mu_{TE}|} \tag{18a}$$

$$\mu_n=\mu_{on}\left(\frac{T_{NOM}}{T}\right)^{|\mu_{TE}|} \tag{18b}$$

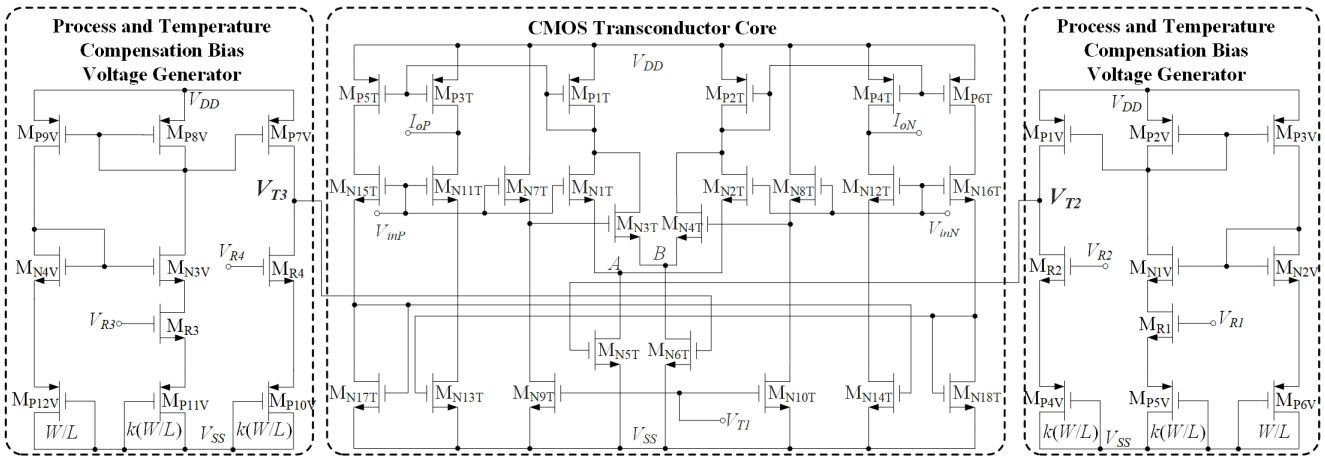

Fig. 3. *The CMOS-level complete schematic of the proposed transconductor*

where μ_{op} and μ_{on} are the hole and electron mobility temperature exponent parameters at the temperature of T_{NOM}; T_{NOM} is the parameter measurement temperature, the default value of which is 27°C; μ_{TE} is the mobility temperature exponent parameter, the default value of which is −1.5.

Now let us take the derivative of μ_n in (18b) with respect to the absolute temperature T, we can get

$$\frac{\partial \mu_n}{\partial T} = \frac{-|\mu_{TE}|\mu_{on} T_{NOM}^{|\mu_{TE}|}}{T^{|\mu_{TE}|+1}} \tag{19}$$

According to (10), (11) and (18a), we can get the derivative of the overdrive voltage of the PMOS transistor operating in subthreshold region with respect to the absolute temperature T

$$\frac{\partial V_{sgt}}{\partial T} = \frac{V_{sgt}}{T} - \frac{nv_t}{T}\left(2-|\mu_{TE}|\right) \tag{20}$$

Now we substitute (19) and (20) into (17), then (17) becomes (21).

Equation (21) gives the temperature coefficient of the transconductor at a given temperature T, which is dependent on the values of V_{sgtP4V} and $V_{sgtP10V}$, the ratio of R_2 to R_1 and the ratio of R_4 to R_3. This means that tuning the ratio of R_2 to R_1 and the ratio of R_4 to R_3 can compensate the process and temperature variations of the transconductor.

We define the voltage parameters of V_{R1}, V_{R2}, V_{R3}, V_{R4} and V_{T1} based on the principle of the flowchart in Fig. 4.

4. Simulation results

The proposed CMOS transconductor is designed in 0.18μm process. The aspect ratios of the MOS transistors in the complete transconductor circuit are listed in Table I. For reducing the transconductance deviation induced by process variations and device mismatch, we choose V_{R1}=V_{R3}=V_{T1}=1.8V. V_{R2} and V_{R4} are generated by the reference voltage divider of Fig.5. Fig. 6 is the layout of the presented transconductor. The transconductor occupies an area of 49×24μm^2. High performance simulations using the Spectre Circuit Simulator have been performed to verify the theoretical analysis.

Table I The aspect ratio of the MOS transistor

MOS transistors	Dimension (W/L)
M_{N1T}-M_{N4T}, M_{N7T}-M_{N18T}, M_{N1V}-M_{N4V}, M_{R1}-M_{R4}, M_{N1D}-M_{N5D}	0.5/0.18μm
M_{N5T}-M_{N6T}	1/0.18μm
M_{P1T}-M_{P6T}, M_{P1V}-M_{P3V}, M_{P6V}, M_{P7V}-M_{P9V}, M_{P12V}, M_{P1D}-M_{P3D}	2/0.18μm
M_{P5D}	3/0.18μm
M_{P4V}-M_{P5V}, M_{P10V}-M_{P11V}	4/0.18μm
M_{P4D}	6/0.18μm

4.1. Verification of the compensation technique of the proposed transconductor

For illustrating the improvement of the proposed transconductor with PT compensation technique, we perform montecarlo simulations to compare the proposed transconductor without (Fig. 1) and with the compensation technique (Fig. 3). The number of samples is 50. Figs. 7a-b show the transconductance variation over temperature (−40-85°C) with process variations and device mismatch. The min ($G_{m,min}$) and max ($G_{m,max}$) statistics of Fig. 7 drawn in Fig. 8 indicate that the transconductance variation ranges of the proposed transconductor without and with PT compensation are equal to 96-140μS and 96-132μS, respectively. Fig. 9 shows that the DC power of the transconductor without and with PT compensation technique equals 1.6-2.8mW and 1.6-2.9mW. Fig. 10 presents the relative deviation error of proposed transconductor (($G_{m,max}$-$G_{m,min}$)/($G_{m,max}$+$G_{m,min}$)) without and with PT compensation technique: 0.8-7.9%, 0.7-5.6%. What's more, we can find that 98% relative deviation error of the proposed transconductor with PT compensation technique is below 5%. However, 26% relative deviation error of the proposed transconductor without PT compensation technique is above 5%. The min and max statistics shown in Fig. 11 present the temperature coefficient of the proposed transconductor without and with PT conpensation technique: ≤1400ppm/°C, ≤900ppm/°C.

$$\frac{\partial G_m}{\partial T} = 2\mu_{on} C_{ox} \frac{W}{L}\left(\frac{T_{NOM}}{T}\right)^{|\mu_{TE}|}\left[\left(|\mu_{TE}|-1\right)\left(\left|\frac{V_{sgtP4V}}{T}\right|+\left|\frac{V_{sgtP10V}}{T}\right|-n\frac{R_2}{R_1}\frac{K_B}{q}lnk-n\frac{R_4}{R_3}\frac{K_B}{q}lnk\right)-2\left(2-|\mu_{TE}|\right)n\frac{K_B}{q}\right] \tag{21}$$

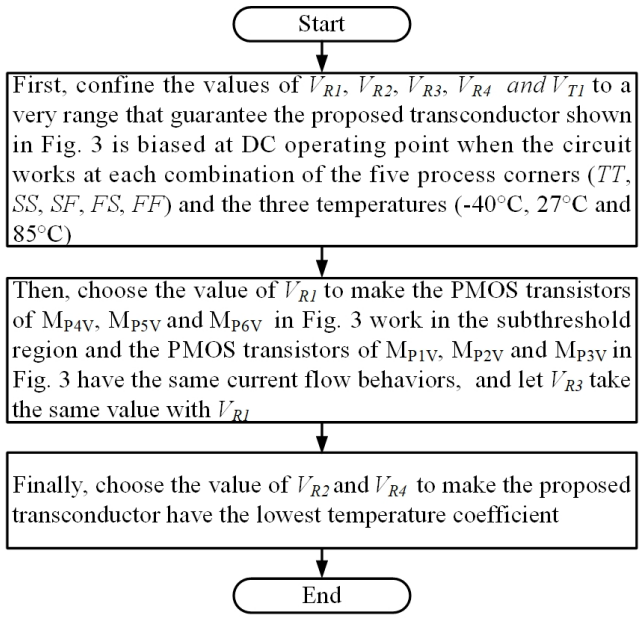

Fig. 4. *The flowchart of how to choose the voltage parameters of V_{R1}, V_{R2}, V_{R3}, V_{R4} and V_{T1}*

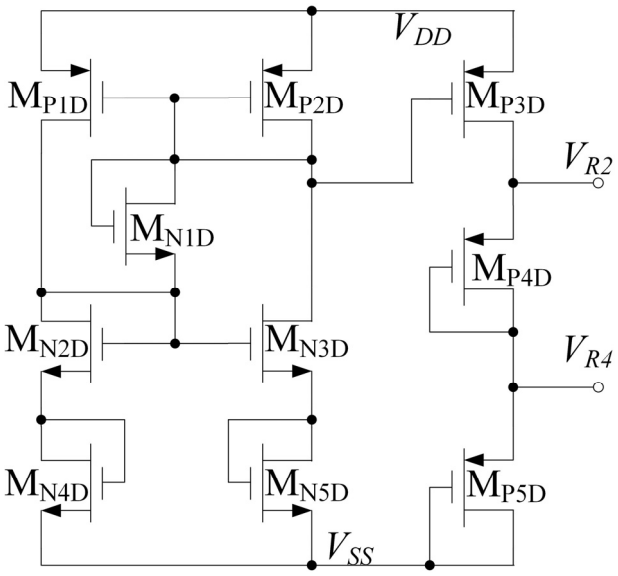

Fig. 5. *Circuit diagram of the voltage reference divider*

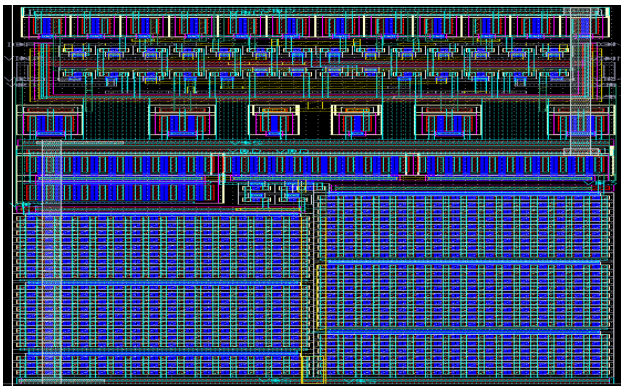

Fig. 6. *Layout of the complete transconductor*

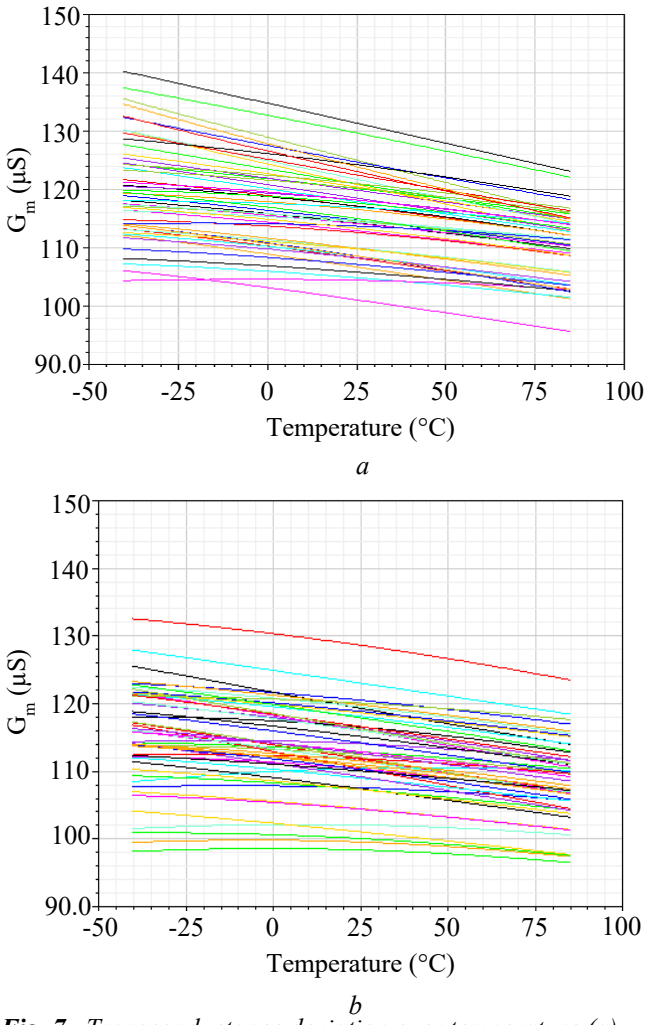

Fig. 7. *Transconductance deviation over temperature (a) without and (b) with PT compensation technique*

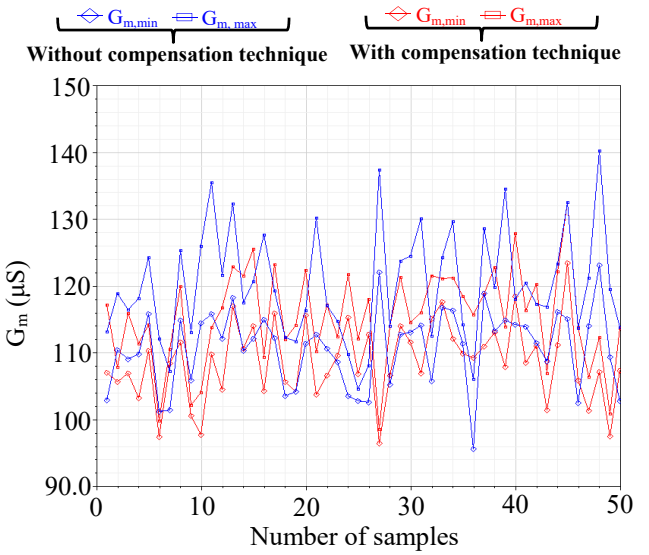

Fig. 8. *The min and max transconductance statistics of the proposed transconductor over temperature*

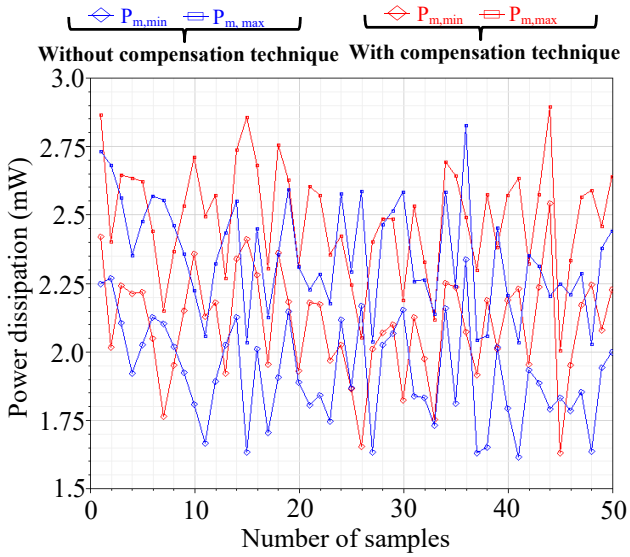

Fig. 9. *The min and max power dissipation statistics of the proposed transconductor over temperature*

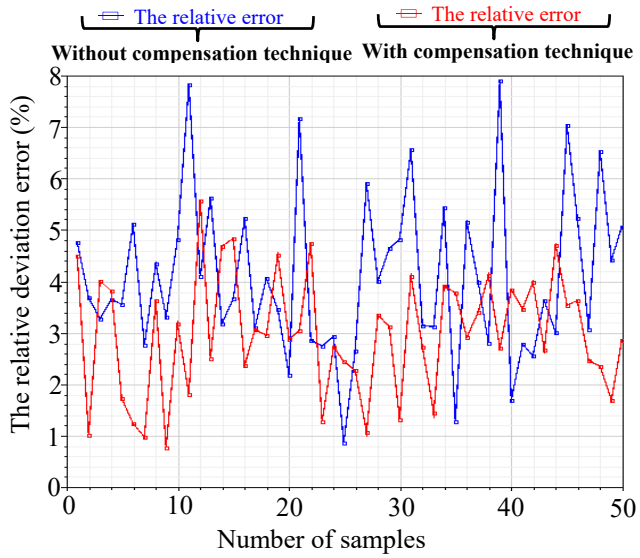

Fig. 10. *The relative deviation error statistics of the proposed transconductor over temperature*

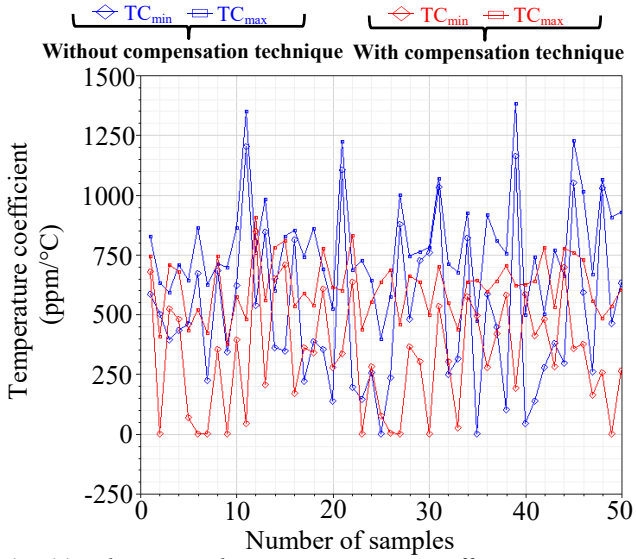

Fig. 11. *The min and max temperature coefficient statistics of the proposed transconductor over temperature*

Table II Performance comparison between the transconductor without and with compensation technique

	Without compensation technique	With compensation technique
Transconductance variation over temperature with process variations and device mismatch	96-140μS	96-132μS
The relative deviation error of the proposed transconductor over temperature	0.8-7.9%	0.7-5.6%
Temperature coefficient of the proposed transcondutor	≤1400ppm/°C	≤900ppm/°C
Power dissipation over temperature	1.6-2.8mW	1.6-2.9mW

Table II summarizes the performance comparison between the proposed transconductor without and with compensation technique. It can be seen that the transcondutor with PT compensation technique has higher tolerance for process and temperature variations than the one without PT compensation technique but hardly consumes more DC power.

4.2. Performance comparison of pre-layout and post-layout simulation

Fig. 12 provides the transconductance variation of the proposed transconductor over temperature for different process corners: 92.3-123.3μS (pre-layout), 91.8-123.6μS (post-layout). Fig. 13 presents the temperature coefficient of the proposed transconductor: ≤1030ppm/°C (pre-layout), ≤1090ppm/°C (post-layout). Fig. 14 shows the DC power dissipation of the proposed transconducor: 1.5-3.3mW (pre-layout), 1.5-3.2mW (post-layout). According to Fig. 15, we can find that the THD of the proposed tranconductor is below -40dB at 1MHz over one sixth the input voltage range. The THD of pre-layout simulation is −82-−72dB at 1MHz for $0.2V_{PP}$ input voltage and the THD of post-layout simulation is −78-−72dB at 1MHz for $0.2V_{PP}$ input voltage. Fig. 16 presents the bandwidth of the transconductor over temperature for different corners: the pre-layout simulation result is from 3.5-7.5GHz, the post-layout simulation is from 2.5-5GHz. Based on Fig. 17, we can get the noise performance of the proposed transconductor: the input referred noise of the pre-layout simulation is from 75.4-125.4nV/sqartHz at 1MHz, the input referred noise of the post-layout simulation is from 78.1-124.8nV/sqartHz at 1MHz. Table III summarizes the performance comparison between pre-layout and post-layout simulation results, from which we can conclude the post-layout simulation results are quite close to the pre-layout.

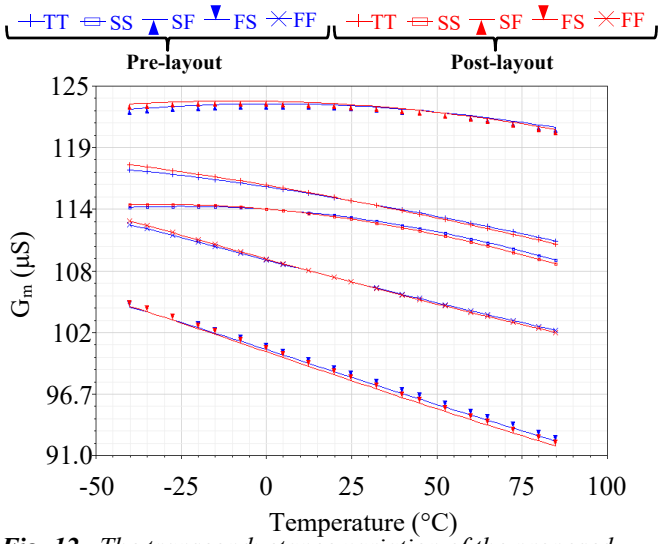

Fig. 12. *The transconductance variation of the proposed transconductor over temperature for different process corners*

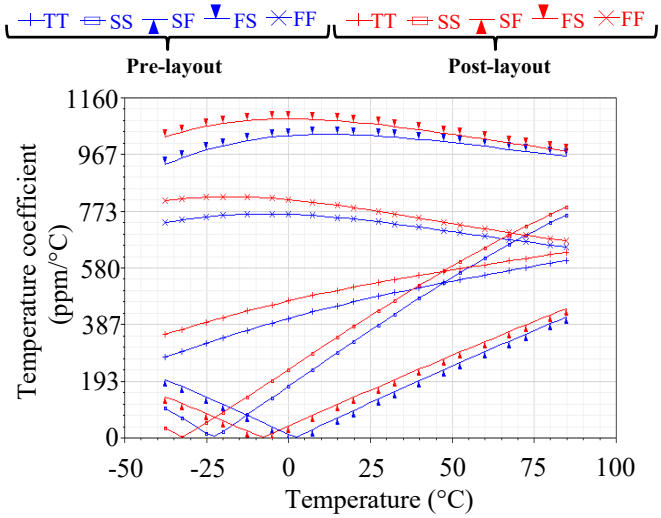

Fig. 13. *Temperature coefficient of the proposed transconductor over temperature for different process corners*

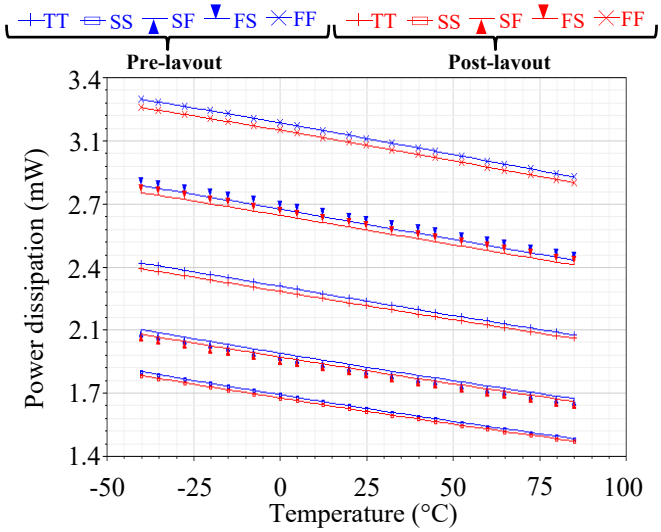

Fig. 14. *Power dissipation of the proposed transconductor over temperature for different process corners*

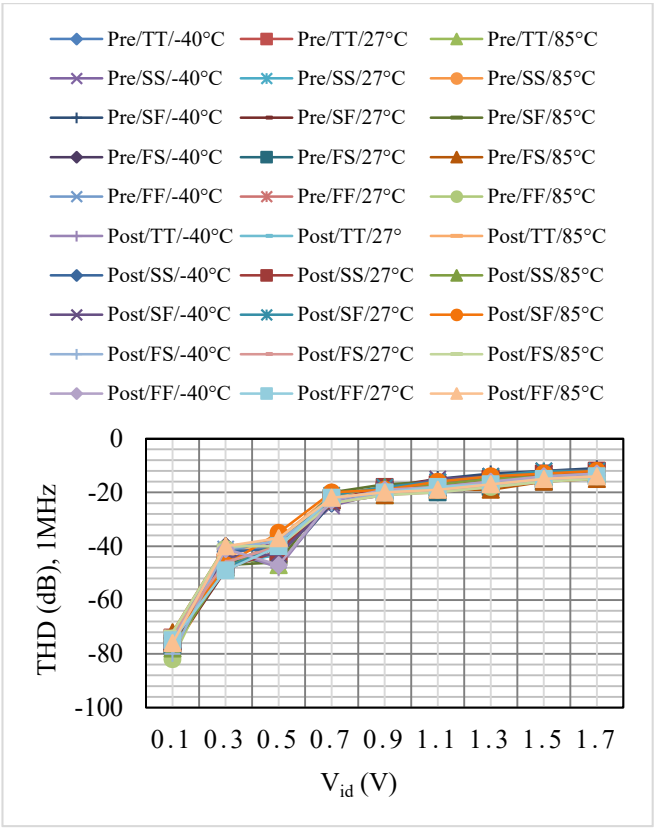

Fig. 15. *Total harmonic distortion of the proposed transconductor at 1MHz over differential input voltage*

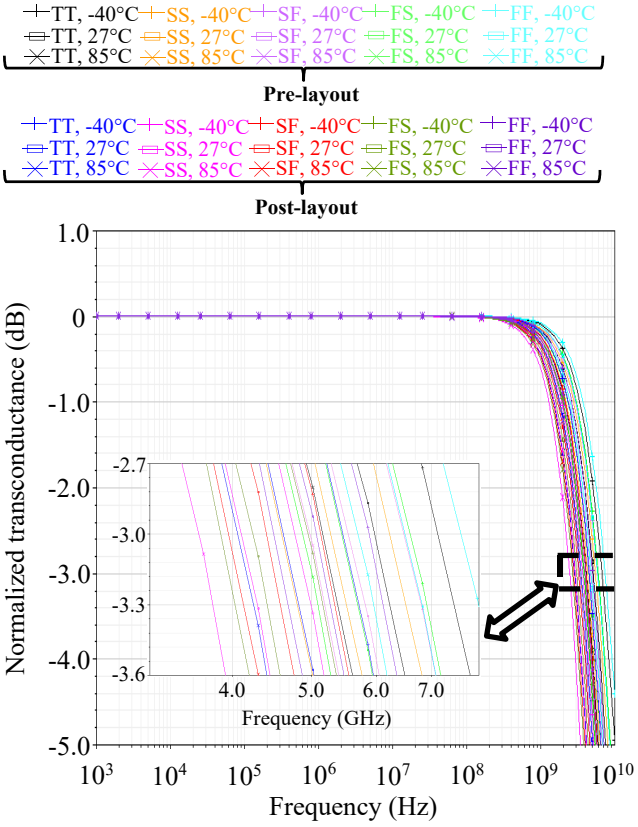

Fig. 16. *The normalized transconductance of the proposed transconductor*

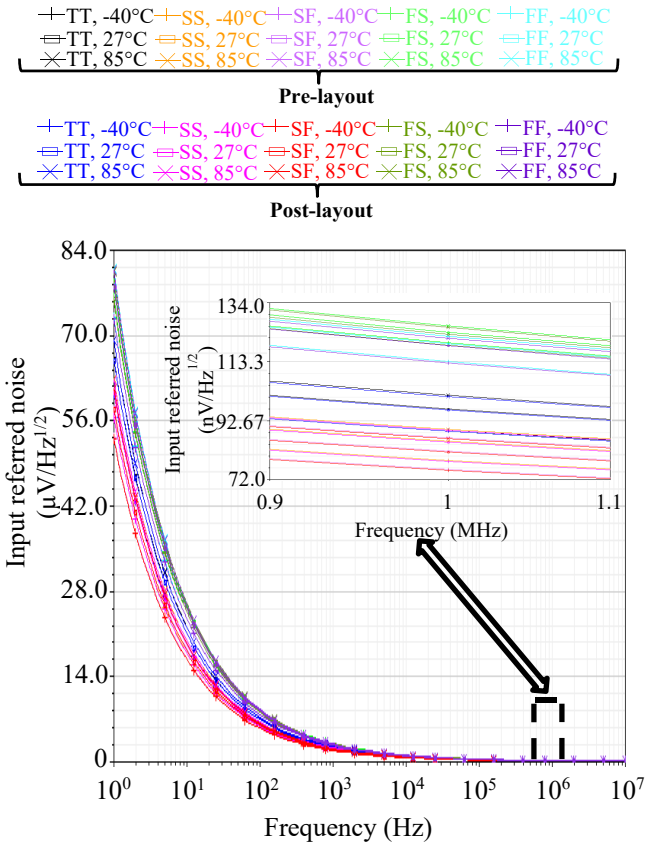

Fig. 17. *The input referred noise of the proposed transconductor*

Table IV compares the performance of the proposed transconductor based on double differential pairs with other types of topology, such as the topologies of source-coupled differential pair [6], cross-coupled differential pair [11], local feedback [12, 17], source degeneration [20], nonlinearity cancellation method [22], the one with PT compensation technique [29], and the pseudo differential pair [13]. The comparison results demonstrate that the proposed transconductor has the lowest temperature coefficient and the second widest bandwidth among the reported works with comparatively low power dissipation and high linearity property. However, the linear input voltage range of the proposed transconductor is narrow, which will be solve in our future work.

5. Conclusions

This paper proposes a novel CMOS transconductor based on a double NMOS transistor differential pairs with process and temperature (PT) compensation technique. The simulation results show that the proposed transconducor has high linearity and strong tolerance for process and temperature variations with relative low power.

6. Acknowledgments

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Table III Performance comparison between pre-layout and post-layout simulation results

	Pre-layout simulation	Post-layout simulation
trans-conductance variation over temperature for different process corner	92.3-123.3μS	91.8-123.6μS
temperature coefficient of the proposed transcondutor	≤1030ppm/°C	≤1090ppm/°C
Power dissipation of the proposed transconductor	1.5-3.3mW	1.5-3.2mW
THD	−82-−72dB @1MHz, 0.2V_{PP}	−78-−72dB @1MHz, 0.2V_{PP}
Bandwidth	3.5 -7.5GHz	2.5 - 5GHz
Input referred noise	75.4-125.4nV/sqartHz @1MHz	78.1-124.8nV/sqartHz @1MHz

Table IV Performance comparison with some reported transconductors

Reference	Algueta, J.M., 2013[6]	Zhao, J., 2017[11]	Acosta, L., 2006[12]	Mondal, I., 2018[17]	Thomas-Erviti, G., 2017[20]	Lewinski, A., 2006[22]	Amarvati, A., 2015[29]	Lujan-Martinez, C., 2008[13]	This work
Type of topology	Source-coupled differential pair	Cross-coupled differential pair	Local feedback	Local feedback	Source degene-ration	Non linearity cance-llation	Process and temperature compensation	Pseudo differential pair	Double differen-tial pair
Technology (μm)	0.5	0.18	0.5	0.13	0.18	0.35	0.18	0.5	0.18
Supply voltage (V)	±1.65	1.8	3.3	1.2	1.8	3.3	1.8	3.3	1.8
G_m (μS)	<55	1.8-31.13	/	12500	/	1200	/	50-200	91.8-123.6
Temperature coefficient (ppm/°C)	/	/	/	/	/	/	14000 /16000	/	≤1090
Linear input voltage range (V)	0.5	0.4	2	0.33	0.2	1.3	/	1	0.2
IM3 (dB)/ THD (dB)	−82 @1MHz, 0.5V_{PP}/	/−48 @1MHz, 0.4V_{PP}	−81dB @10MHz, 2V_{PP}/−91 @10MHz, 2V_{PP}	/−40 @1MHz, 0.33V_{PP}	/−72 @100KHz, 0.2V_{PP}	−70 @70MHz, 1.3V_{PP} /	/	−71dB @1MHz, 1V_{PP}/−78 @1MHz, 1V_{PP}	/−78-−72 @1MHz, 0.2V_{PP}
-3dB bandwidth (MHz)	/	185-1610	/	20000	/	/	/	40	2500-5000
Input referred noise (nV/sqartHz)	/	/	/	1.75	/	7	/	61@5MHz	78.1-124.8 @1MHz
Power consumption (mW)	/	0.009-0.14	0.4125	5.5	0.054	9.5	0.136	1.25	1.5-3.2

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