xDSL Network Upgrade Employing FPGAs

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Abstract

This paper proposes an upgrade scenario for xDSL networks to provide broadband access for extended link lengths while demonstrating network grooming by means of more than one subscriber using a single network connection concurrently. This is achieved by applying Direct Spread Code Division Multiple Access (DS-CDMA) in a Fiber-to-the-Cabinet (FTTC) topology by means of a Field Programmable Gate Array (FPGA), used to demonstrate simultaneous user transmission and System-on-Chip (SoC) network element generation. Experimental results have displayed efficiency in ADSL link rates of 66% and 41% for back-to-back and 12km-reach fiber links respectively.

1. Introduction

BANDWIDTH demand in access networks is constantly increasing to support the application of new services expected to extend subscriber requirements in bandwidth by up to 100 Mbps in the medium future [1, 2]. Consequently, telecom operators are faced with several techno-economical challenges to provide broadband access in an efficient and profitable manner over an extended-reach local loop network. Among the access architectures proposed to demonstrate future bandwidth-intensive, service-aware networks, fibre-to-the-home (FTTH) has been nominated as the ultimate topology to provide thick bandwidth pipes all the way to the end users [3, 4]. However, due to high capital and operational costs associated with FTTH, an alternative approach has been widely supported and increasingly deployed to demonstrate deep-fiber penetration [5] in conjunction with x-digital subscriber line (xDSL) signalling distributed from an access node to the customer premises equipment (CPE).

Research initiatives in reducing the bandwidth limited copper-based local loop and subsequently provide extended link servicing, have proposed the application of subcarrier multiplexing (SCM) [6]. In this approach, different subcarriers are assigned to integrate individual DSL channels over a common optical fiber carrier scheduled in a fibre-to-the-cabinet (FTTC) topology. The drawback of this approach is that spectrum is not utilised efficiently since adding new users would require further subcarriers, thus requiring increased transmission bandwidth. In addition, multiple local oscillators are required to modulate the network subcarriers increasing the system complexity and cost [6].

In this paper an alternative architectural approach is proposed to demonstrate the feasibility of an xDSL network providing significantly increased overall loop link lengths and effective line rates. This is achieved by employing Direct Spread Code Division Multiple Access (DS-CDMA) to encode multiple Discrete Multi Tone (DMT) channels by means of a Field Programmable Gate Array (FPGA) device used for code generation and cabinet System-on-Chip (SoC) integration. Multiple DSL channel encoding over a single FPGA offers network scalability since new subscribers can be easily integrated by simply reprogramming the array. The use of the FPGA also offers in-field SoC implementation reducing the cabinet complexity cost and size.

In section 2 of this paper the proposed network architecture is presented with the FPGA initially limited to code generation for spreading the DMT channels, following analogue transmission over the fibre link length. As a result, section 4 introduces digital transmission where the FPGA is proposed to implement an all-digital cabinet to multiplex the DMT channels before being transmitted over the fiber link and routed through the Digital Subscriber Line Access Multiplexer (DSLAM) at the local exchange.

2. Proposed Network Architecture

The proposed network shown in figure 1 consists of
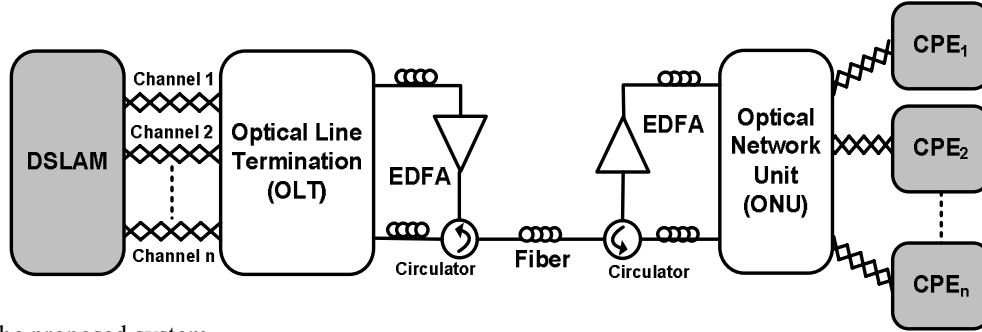
Figure 1: The proposed system

an asymmetric-DSL2+ (ADSL2+) modem at the customer premises equipment (CPE) connected via a typical unshielded twisted pair (UTP) cable to a street cabinet comprising an optical network unit (ONU). In the ONU, multiple ADSL2+ channels are multiplexed using DS-CDMA and transmitted over a standard single mode fiber (SSMF) at the end of which they are demultiplexed in the OLT located in the local exchange. After demultiplexing, an ADSL2+ compatible DSLAM receives all subscribers' traffic. The proposed network elements representing the ONU and OLT are shown in figures 2 and 3, respectively.
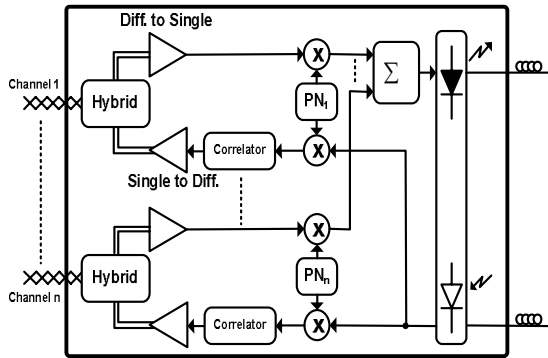
Figure 2: OLT for n users
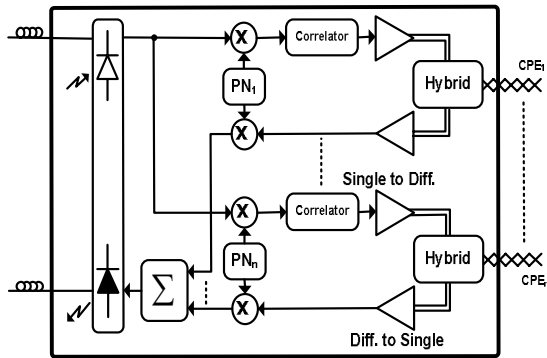
Figure 3: ONU for n users

In downstream the UTP input ports to the OLT, shown in figure 2 at the output of the DSLAM, comprise of n active hybrids to allow bidirectional signal transmission. Each hybrid can be designed using transformers, operational amplifiers or directional couplers [6]. Hybrids based on operational amplifiers are used in this study since they have been shown to outperform their counterparts by providing higher isolation in the return direction [6].

The analogue differential output from the hybrid is converted to single-ended using a differentiator before being multiplied with a Gold pseudo-random (PN) sequence generated in the FPGA to display superior correlation [7]. This is achieved by designing two sets of shift registers from the preferred pairs of m-sequences. The number of shift registers in each set depends on the period of the required code. Both sets are then X-ORed bit by bit, producing the required Gold code at the output. At this stage the Xilinx ISE platform was used to upload the generated codes on the FPGA. It should be noted that in order to generate multiple codes only the initial conditions of the shift registers have to be changed.

The application of the FPGA was initially selected due to its inherited scalability, dynamicity and flexibility to implement, reconfigure and increase the number of the Gold codes to improve network penetration by means of software modifications. After supplying each ADSL2+ channel with a unique code, the coded channels were superimposed and direct modulated a distributed feedback laser (DFB) diode at 1550 nm and 0 dBm. A circulator is used after the DFB laser to allow bidirectional transmission.

In the ONU the signal from the output of the circulator is detected initially by a photodiode and subsequently multiplied with the same Gold code. Any interference caused by the multiple users is reduced using a correlator thus increasing Signal-To-Noise ratio (SNR). The output of the correlator is finally converted back to differential and applied to the

hybrid to allow transmission over the UTP cable all the way to the CPE.

3. Experimental Results

To evaluate the system performance, 10 Mbps Gold codes with 1024 bits period were initially considered to exhibit sufficient processing gain in parallel with high efficiency at the CDMA decoder by means of decreased computational time. To demonstrate the architecture's feasibility to provide each subscriber ADSL2+ compatible downstream rates for much longer distances compared to the standard [8], the bit loading of a single CDMA-encoded channel was investigated in downstream with no error correction applied to present the worst case scenario.

Figure 4 displays the bit loading of the downstream DMT tones over 2.2 MHz bandwidth with the OLT output connected directly to the ONU input and therefore bypassing the fiber transmission medium to monitor the system's back-to-back performance. The recorded transmission rates and link lengths achieved under this set-up are expected to form a reference for comparison for future experiments when a complete network comprising of multiple users located at several kilometres away from the local exchange will be investigated.
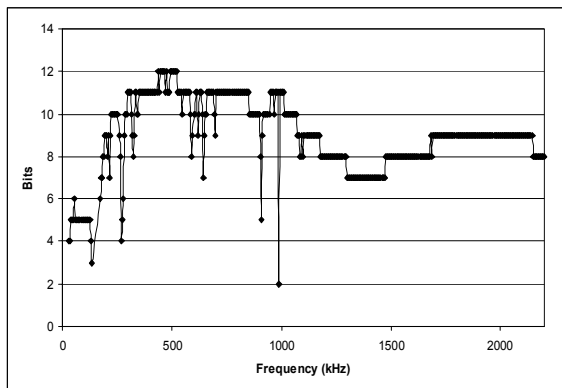

Figure 4: Bit loading in back-to-back transmission

As shown in figure 4 the maximum number of bits allocated for those tones above 1 MHz is approximately 9 in comparison to lower frequency tones for which the maximum number of allocated bits is 12. This characteristic is expected since higher frequency tones tend to suffer from extended attenuation. In contrast, the total number of bits per tone in a practical system with typical SNR in the range of 10-20 dB is expected to be higher. The application of linear mixers to encode and decode the

ADSL2+ channels and effective termination between the FPGA and analogue printed circuit board is expected to improve the system loading. In addition, the complete implementation of the cabinet electronics over an FPGA is expected to enhance network performance since lower noise figures are predicted due to the elimination of analogue processing.

Closed loop point – to – point test implementations by means of the DSLAM inherited diagnostic software have displayed maximum attainable downstream data rates of 16 Mbps corresponding to 66% link rate efficiency in comparison to equipment specifications. Although this is expected to increase for the reasons already stated, the monitored efficiency is similar to the figure achieved with the SCM approach [6].

Further experimentations were conducted to monitor the system performance in the presence of a 12 km fiber reel with no amplification, consisting of standard SSMF to represent the range of deployed FTTC architectures. The corresponding bit loading, shown in figure 5, displays a maximum of 7 bits assigned to the higher SNR tones at the upper end of the ADSL2+ spectrum achieving a total downstream rate of up to 10 Mbps. Subsequently the obtained modem efficiency reached up to 41%.
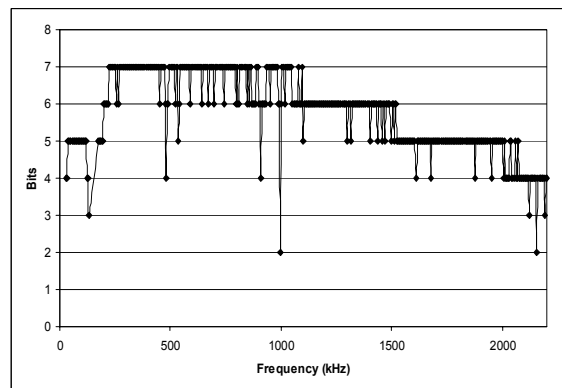

Figure 5: Bit loading with 12km fiber

4. All-digital FPGA-based Cabinet

In this section, the application of the FPGA is proposed to implement an all-digital CDMA encoder and decoder in the network cabinet. This is expected to reduce the system complexity, increase its performance by reducing processing noise and backreflections, in terms of misterminations, and increase the cabinet dynamicity by means of the superimposed programmability of the FPGA.

As illustrated in figures 6 and 7, the output from the differential to single-ended converter from each

ADSL2+ channel in downstream is applied to an Analogue-to-Digital (A/D) converter and fed to the FPGA. In the FPGA, in addition to the Gold codes described in section 2, a complete CDMA encoder is developed to perform digital spreading of each user data. Following the addition of all coded channels, the composite output of the programmable array was used to modulate a DFB laser with the same specifications as before.

In upstream the output from the photodiode is fed to the CDMA decoder compiled in the same FPGA, as shown in figure 7, to correlate the received data with the synchronised replica of the user code. The output from the decoder is then fed to the digital-to-analogue (D/A) converter and applied as the return signal to the single-to-differential converter.
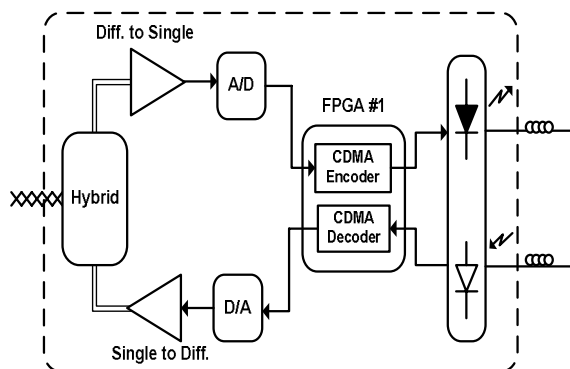

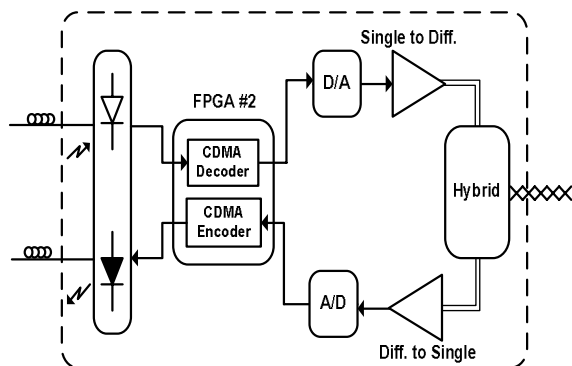**Figure 6:** Digital Optical Line Termination (OLT)

Figure 7: Digital Optical Network Unit (ONU)

To demonstrate the developed network performance, a simple system based on the architectural approach described in section 2 is implemented and transformed to include the new elements. As can be seen from the experimental set-up of figure 8, the DMT ADSL2+ signal in downstream is initially converted to digital and after performing signal processing in the FPGA the resulted signal is

converted back to analogue and fed through the hybrid to the user modems. For the purpose of the experimentations, the upstream propagation is bypassed using a Low Pass Filter (LPF) to avoid smearing of any portion of the downstream signal through the hybrid to the upstream.
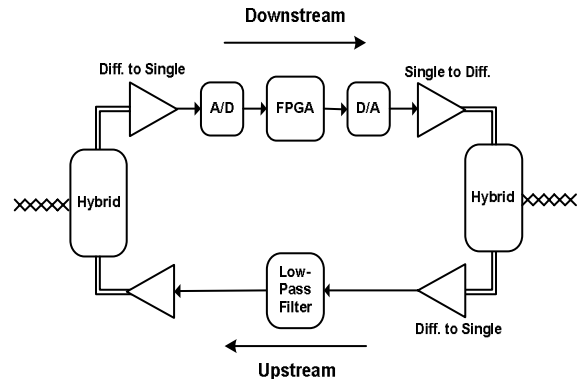

Figure 8: The implemented FPGA based system

4.1. FPGA Implementation

The FPGA schematic, shown in figure 9 has been implemented using Handel-C and compiled using DK version 4 (DK4) on the RC10 board. Handel-C is a high level language that is at the heart of a hardware compilation system known as Celoxica Development Kit (DK) [9]. This is designed to compile programs written in a C-like high level language into synchronous hardware [10]. DK produces a Netlist file, which is used during the place and route stage to generate the image or bit stream file [9]. The RC10 board is fitted with a 1.5 million-gate Xilinx Spartan 3 FPGA and is packaged with a set of comprehensive support libraries intended for use with Celoxica's DK Design Suite. The board is packed with a powerful set of I/O features including two high speed 10-bit A/D converter channels and each channel has its own set of pins on the FPGA [8].

Figure 9 illustrates the possible implementation of the DS-CDMA encoder and decoder without the transmission channel. The encoding and decoding process follows the same principle as discussed before. However, the complete CDMA system is now implemented using the FPGA. The X-OR gates are used in place of the multipliers. The output from the high data rate PN generator is X-ORed with the lower data rate output from the A/D converter resulting in the spread spectrum.

In order to recover the original signal the coded output is fed to another X-OR gate that is usually placed at the receiver. Parallel X-ORing is used.
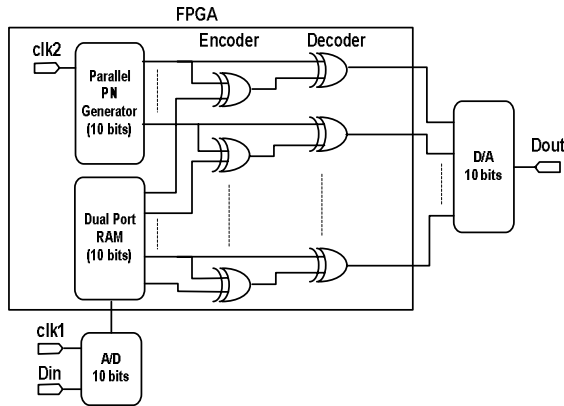
Figure 9: DS-CDMA implementation on FPGA

The samples from the A/D are stored in a Dual Port RAM and the parallel PN generator is implemented using Xilinx's CoreGen utility, which contains many designs to save programming time [10].

Since the PN runs with a higher data rate, the two clock domains approach, shown in figure 10, is used. Communication between the two domains is allowed through the use of a channel and a dual port RAM. Using a channel in Handel-C ensures that any data will always be transmitted accurately between clock domains and avoids problems with metastability that can occur when communicating between each other.
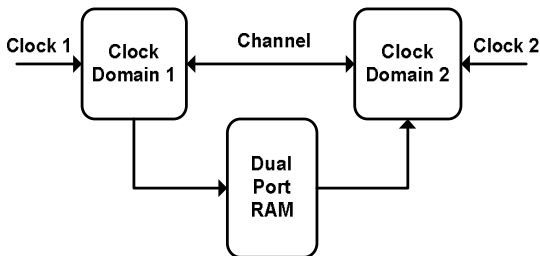
Figure 10: Multiple clock domain

The aim of the future work is to digitally implement the entire system by using two FPGAs at the ONU and OLT levels. In addition, and due to increasingly tighter power budgets, the issues of power consumptions will be tackled by looking at techniques for minimising it at the algorithm and architectural level while maintaining other competitive performance metrics.

5. Conclusion

This paper presents an upgrade scenario for xDSL networks based on DS-CDMA to demonstrate multiple xDSL user transmission over extended local loop link lengths based on standard SSMF. This was achieved by the use of an FPGA in a FTTC architecture to ultimately implement an all-digital processing array in the network ONU offering reconfigurability for simple network scaling. The successful transmission of a coded ADSL2+ channel in back-to-back and 12-km optical fiber configurations with 66% and 41% obtained efficiency in ADSL2+ link rates respectively has demonstrated the feasibility of an inexpensive fiber-extended xDSL programmable networks with no extra requirements in transmission bandwidth. Depending on vigilant redevelopment, this architecture can provide an important staging post on the carriers' path to FTTH.

6. References

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